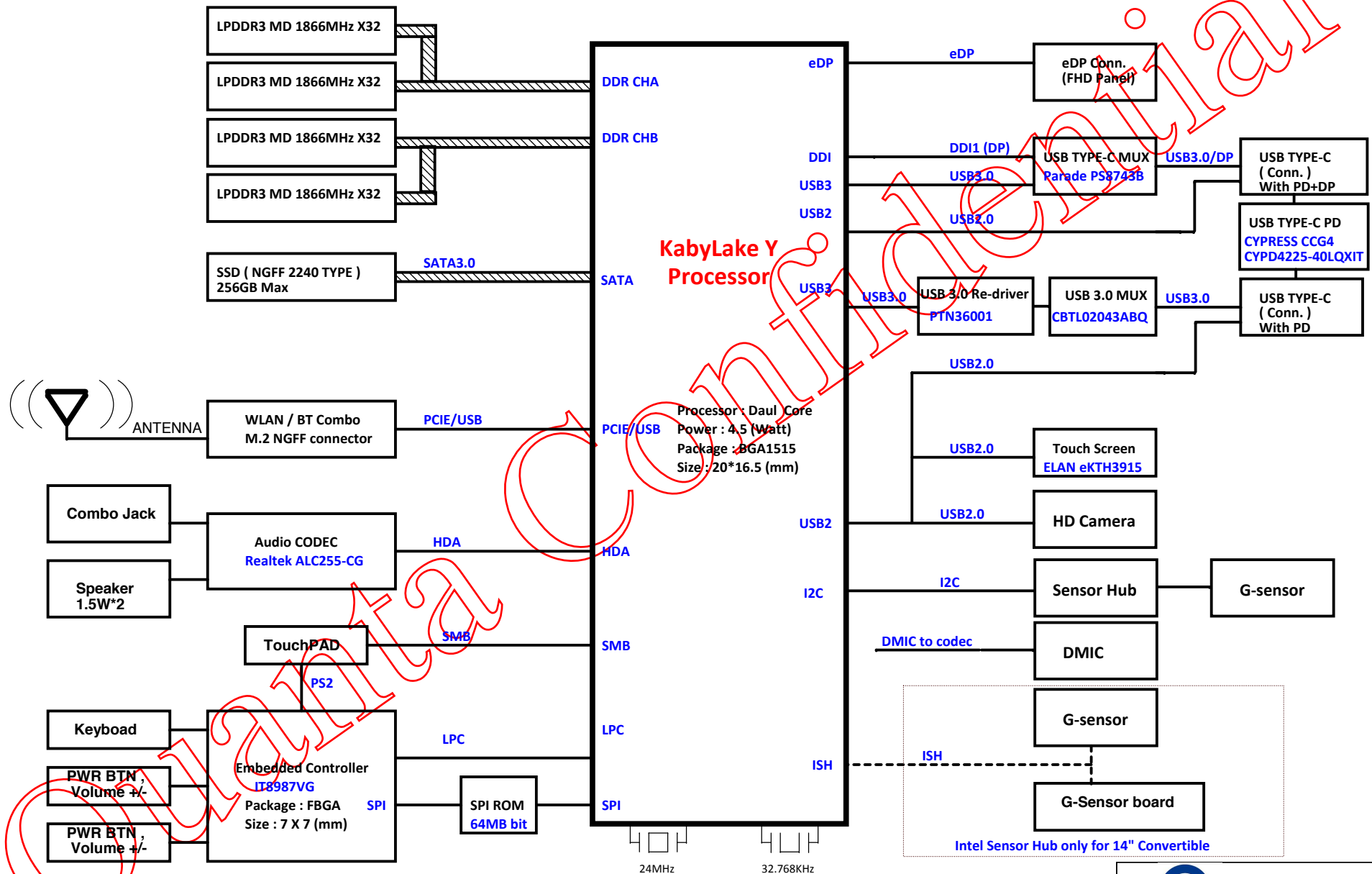
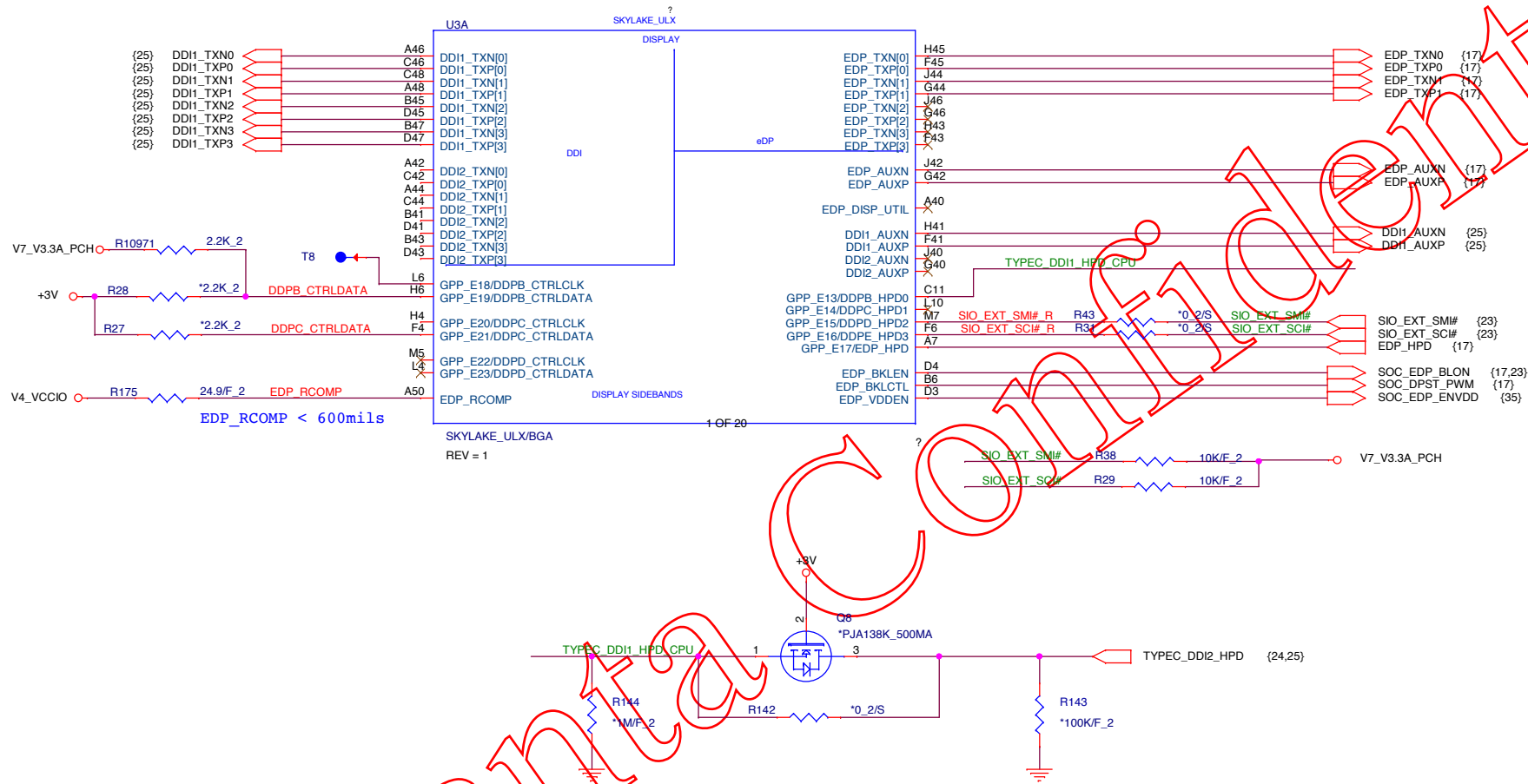


Block Diagram

01

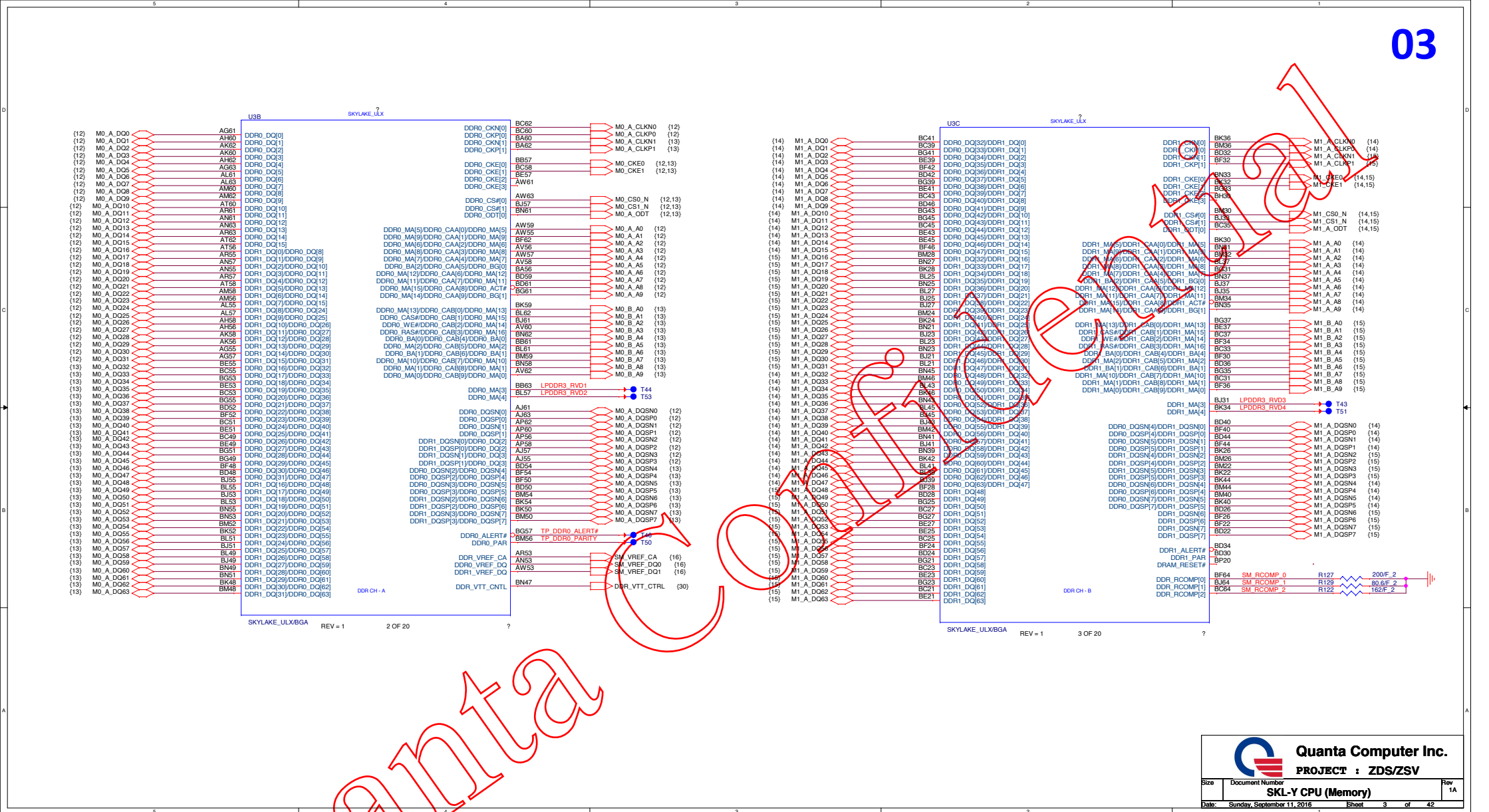




Quanta Computer Inc.

PROJECT : ZDS/ZSV

Size	Document Number	Rev
	SKL-Y CPU (DDI/EDP)	1A
Date:	Sunday, September 11, 2016	Sheet 2 of 42

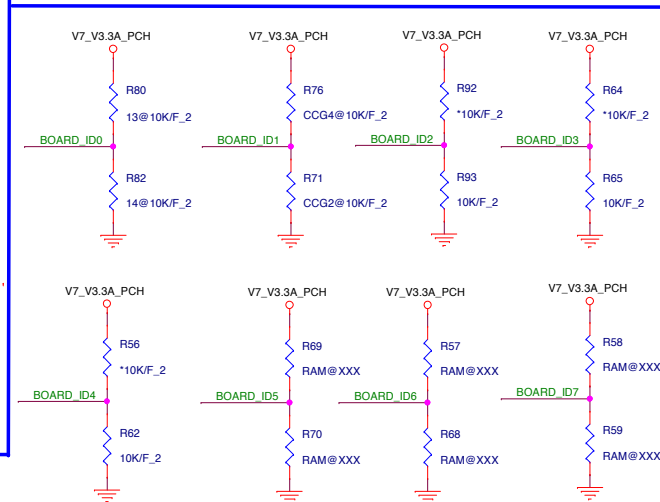
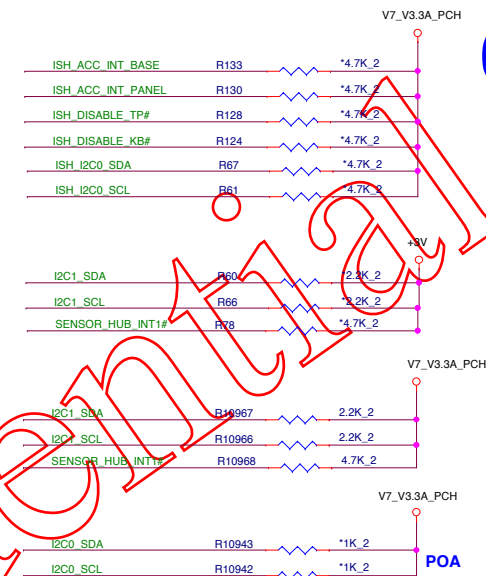




USB Type C adapter

+VCCST_CPU
Ω

Date: Sunday, September 11, 2016 Sheet 4 of 42



Board ID Reserve		
ZDS ZDV	H L	ID0
SKL-Y KBL-Y	H L	ID1
Reserve	H L	ID2
Reserve	H L	ID3
Reserve	H L	ID4

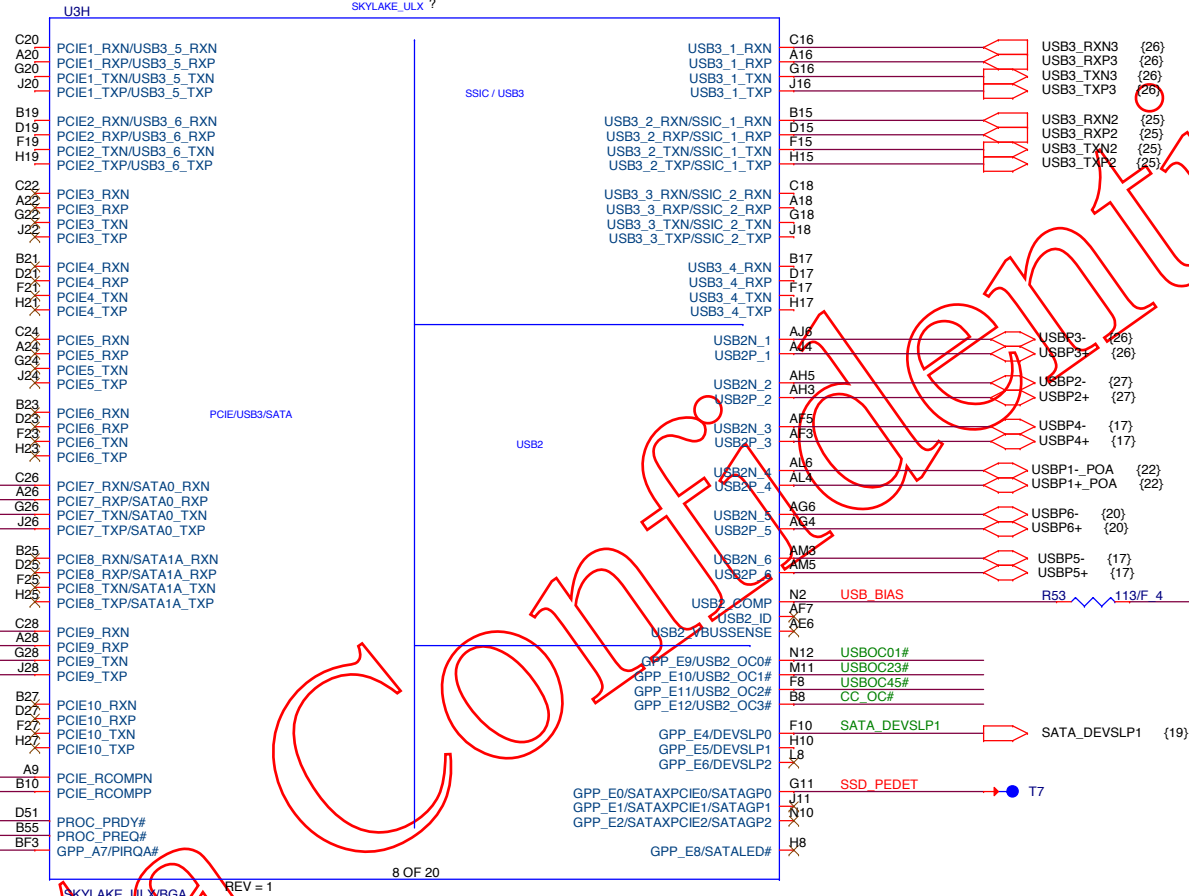
SATA_SSD

WLAN

(19) SATA_RXN
(19) SATA_RXP
(19) SATA_TXN
(19) SATA_TXP

{20} WLAN_PCIE_RXN9
{20} WLAN_PCIE_RXP9
{20} WLAN_PCIE_TXN9
{20} WLAN_PCIE_TXP9

R35 100/F_2
T9 XDP_PRDY#
T13 XDP_PREQ#
PIRQA#



TYPE-C port1 for PD

TYPE-C port2 for PD+DP

TYPE-C port1 for PD

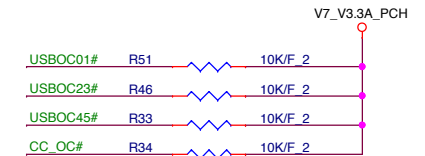
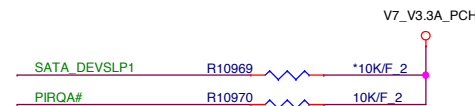
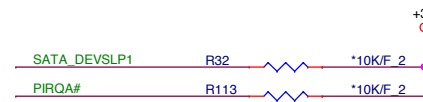
TYPE-C port2 for PD+DP

CCD

POA

WLAN BT

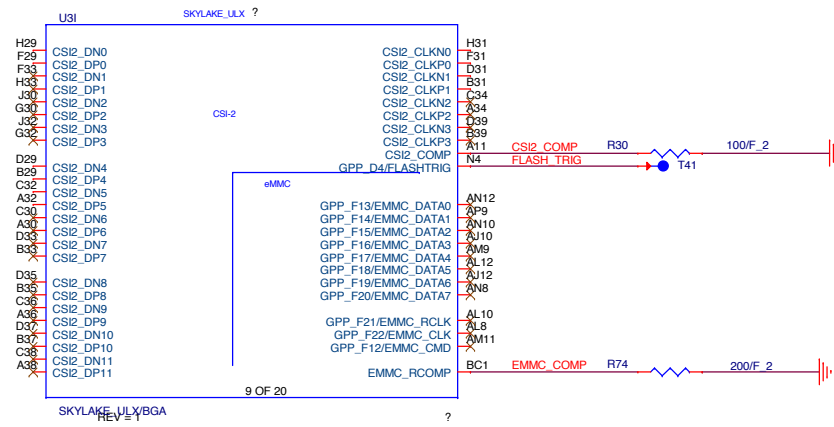
Touch Screen



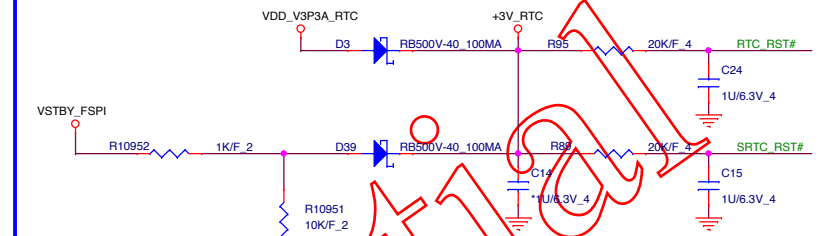
Quanta Computer Inc.

PROJECT : ZDS/ZSV

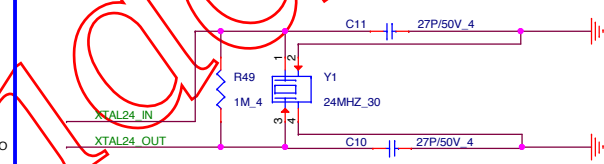
Size	Document Number	Rev
	SKL-Y CPU (PCIE/USB3)	1A
Date:	Sunday, September 11, 2016	Sheet 6 of 42



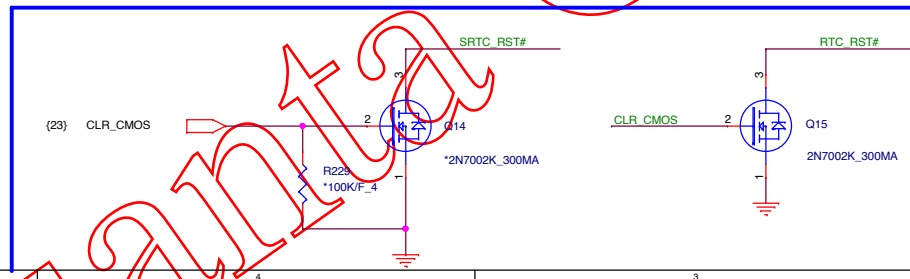
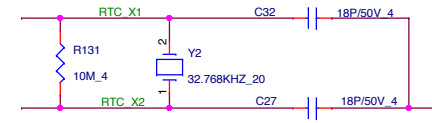
RTC Circuitry(RTC)

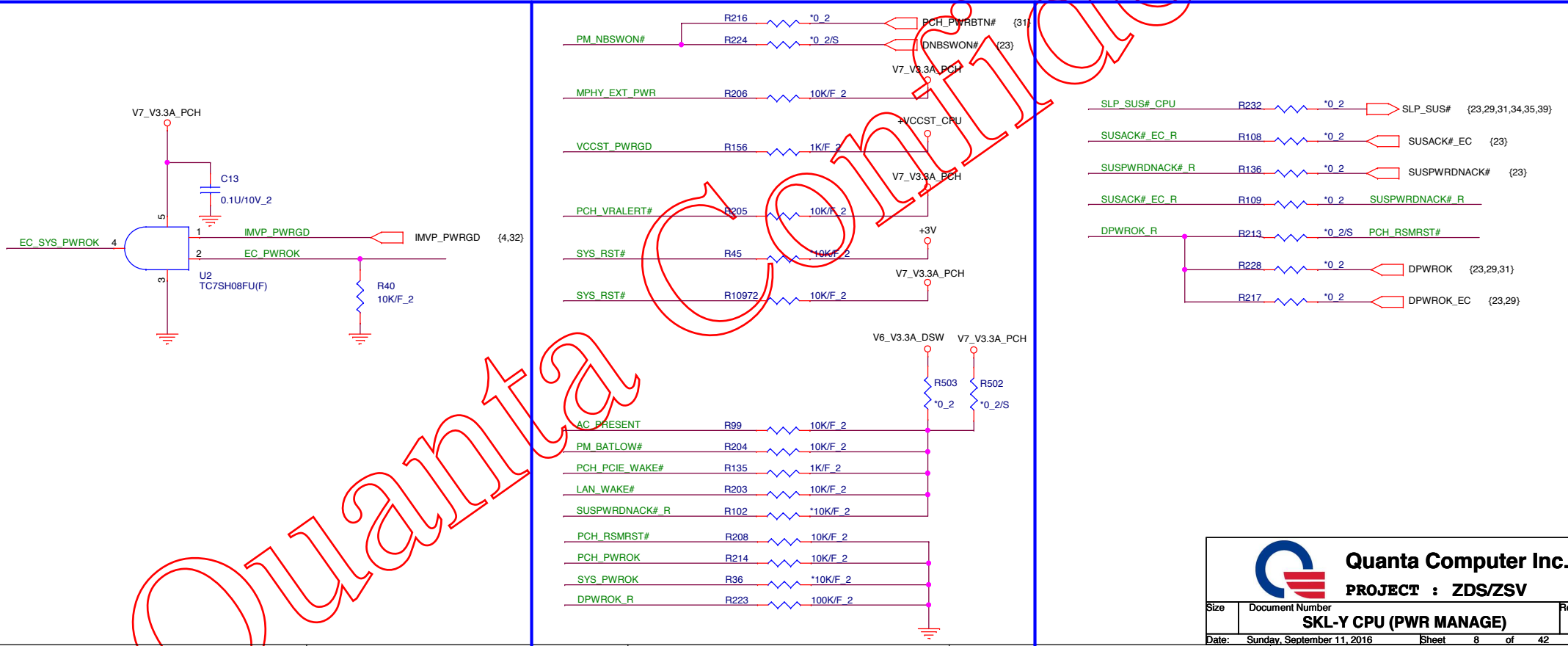
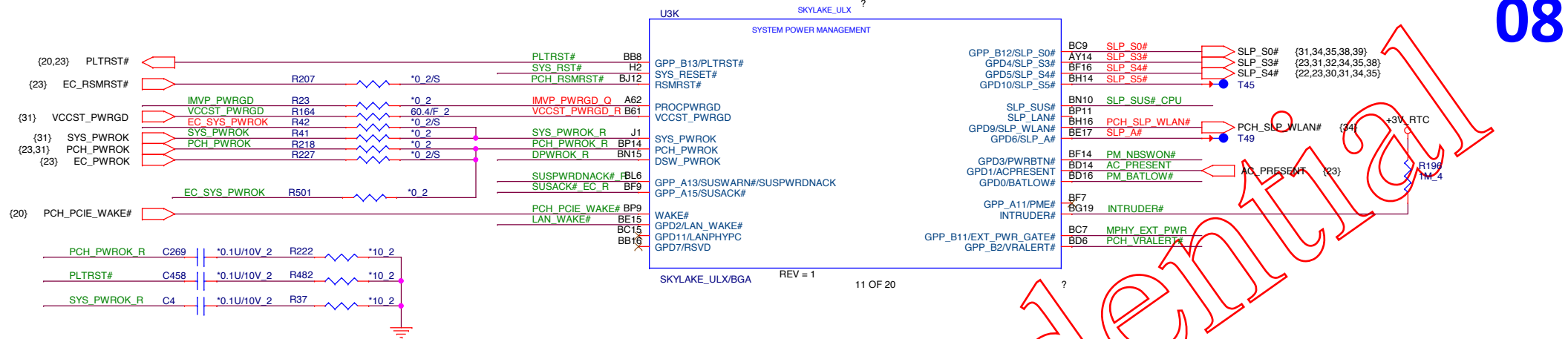


PCH Crystal (CLG)



RTC Crystal (CLG)



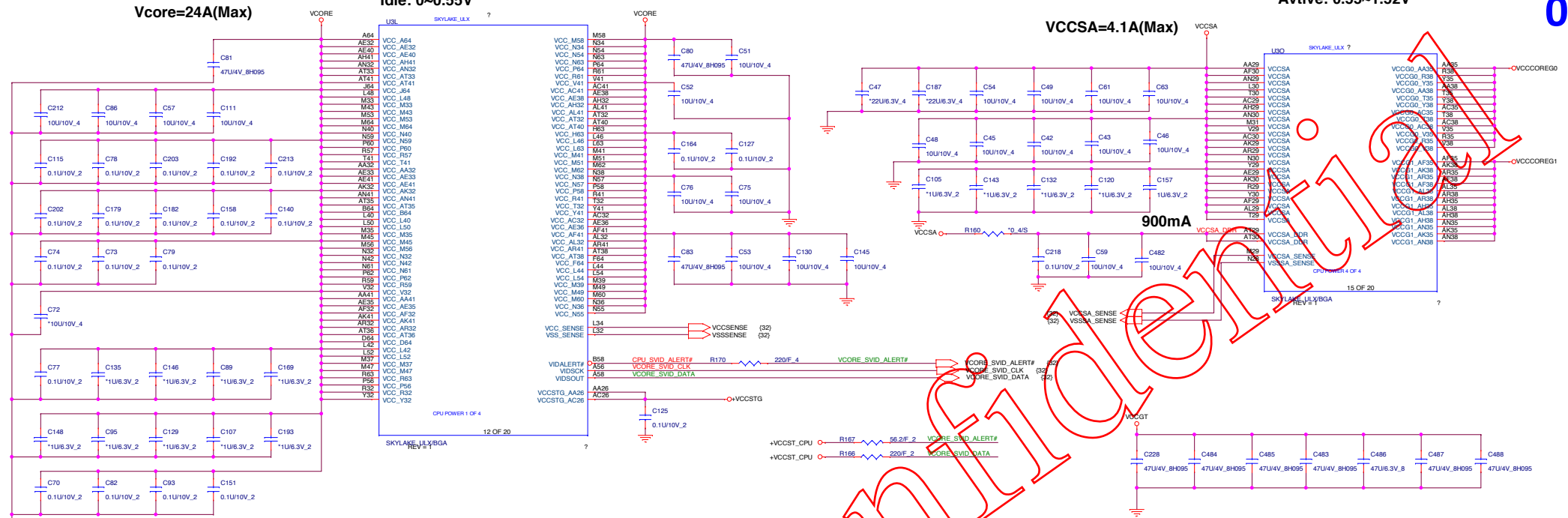


Quanta Computer Inc.
PROJECT : ZDS/ZSV

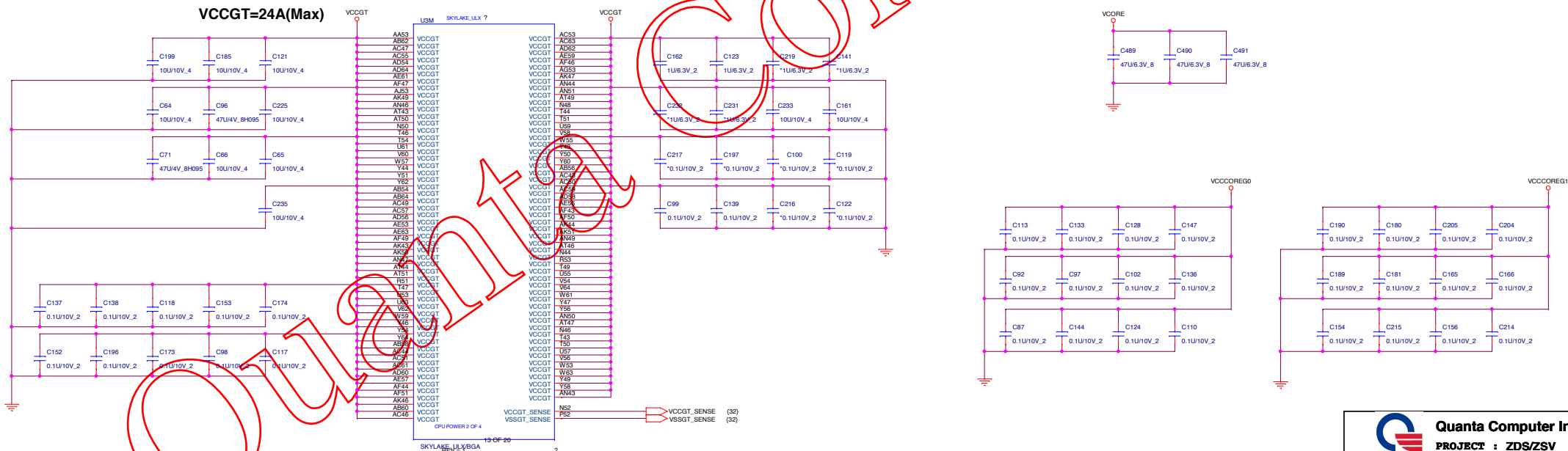
Size	Document Number	Rev
	SKL-Y CPU (PWR MANAGE)	1A
Date:	Sunday, September 11, 2016	Sheet 8 of 42

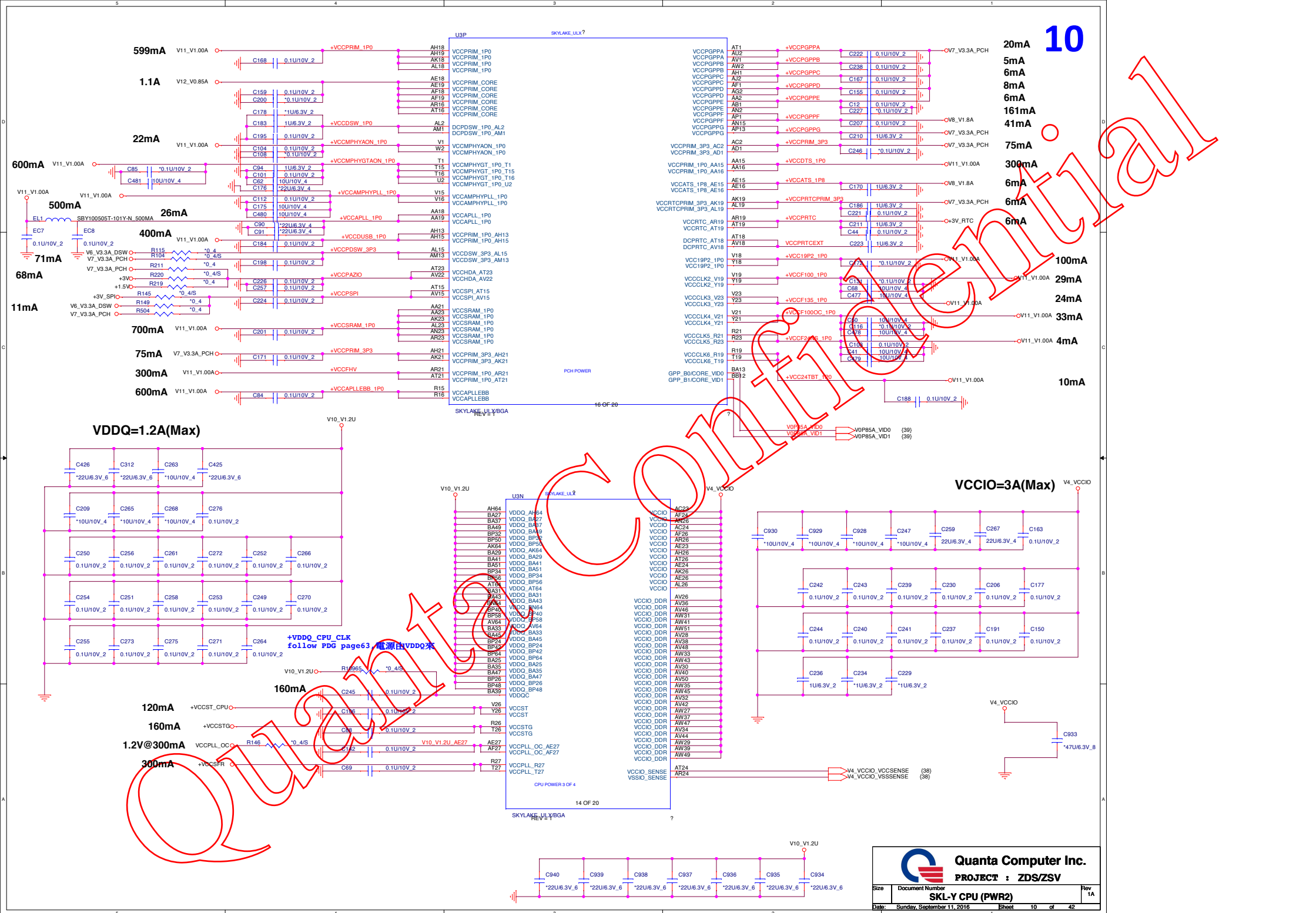
Active: 0.55~1.52V
Idle: 0~0.55V

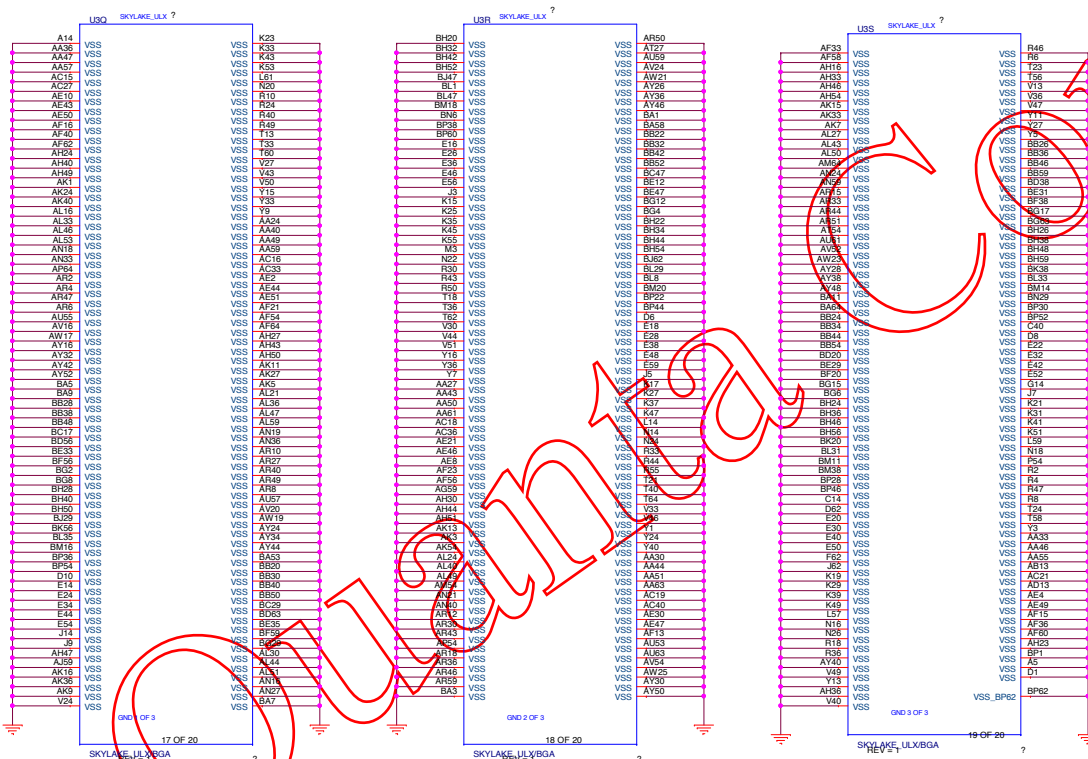
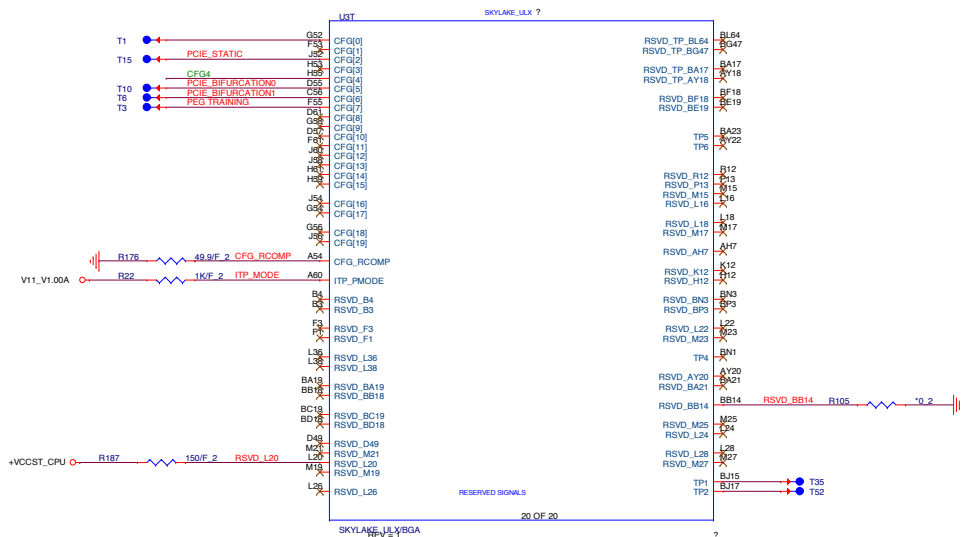
Active: 0.55~1.52V



Active: 0.55~1.52V
Idle: 0~0.55V







Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = Normal Operation 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = Normal Operation 0 = Lan number reversed	
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled 0 = Enabled	
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express 01 = Disabled 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	
CFG[7]	PEG Training	1 = *PEG Train immediately follow RESET# de-assertion 0 = PEG wait for BIOS for training	
CFG[19:8]	Reserved Configuration lane		
SPKR / GPP_B14	Top-Block Swap Override	1 = Enable 0 = Disable	
BSPI0_MOSI / GPP_B18	No Reboot	1 = Enable 0 = Disable	
SMBALERT# / GPP_C2	eSPI or LPC	1 = Enable 0 = Disable	Reserve Pull-high on Page.4
Boot BIOS Strap Bit / GPP_B22	Boot BIOS Strap Bit (BBS)	1 = LPC 0 = SPI	default:SPI
SML0ALERT# / GPP_C5	eSPI or LPC	1 = eSPI 0 = LPC	Reserve Pull-high on Page.4 (default:LPC)
SML1ALERT# / PCNHOT# / GPP_B23			Reserve Pull-high on Page.6
SPI0_MOSI			Reserve Pull-high on Page.4
SPI0_MISO			Reserve Pull-high on Page.4
SPI0_IO2			Reserve Pull-high on Page.4
SPI0_IO3			Reserve Pull-high on Page.4
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override	1 = Disable 0 = Enable	
DDPB_CTRLDATA / GPP_E19	Port B Detected	1 = Enable 0 = Disable	Already Pull-high on Page.2
DDPC_CTRLDATA / GPP_E21	Port C Detected	1 = Enable 0 = Disable	Reserve Pull-high on Page.2

LPDDR3 MEMORY CHANNEL A-1

12

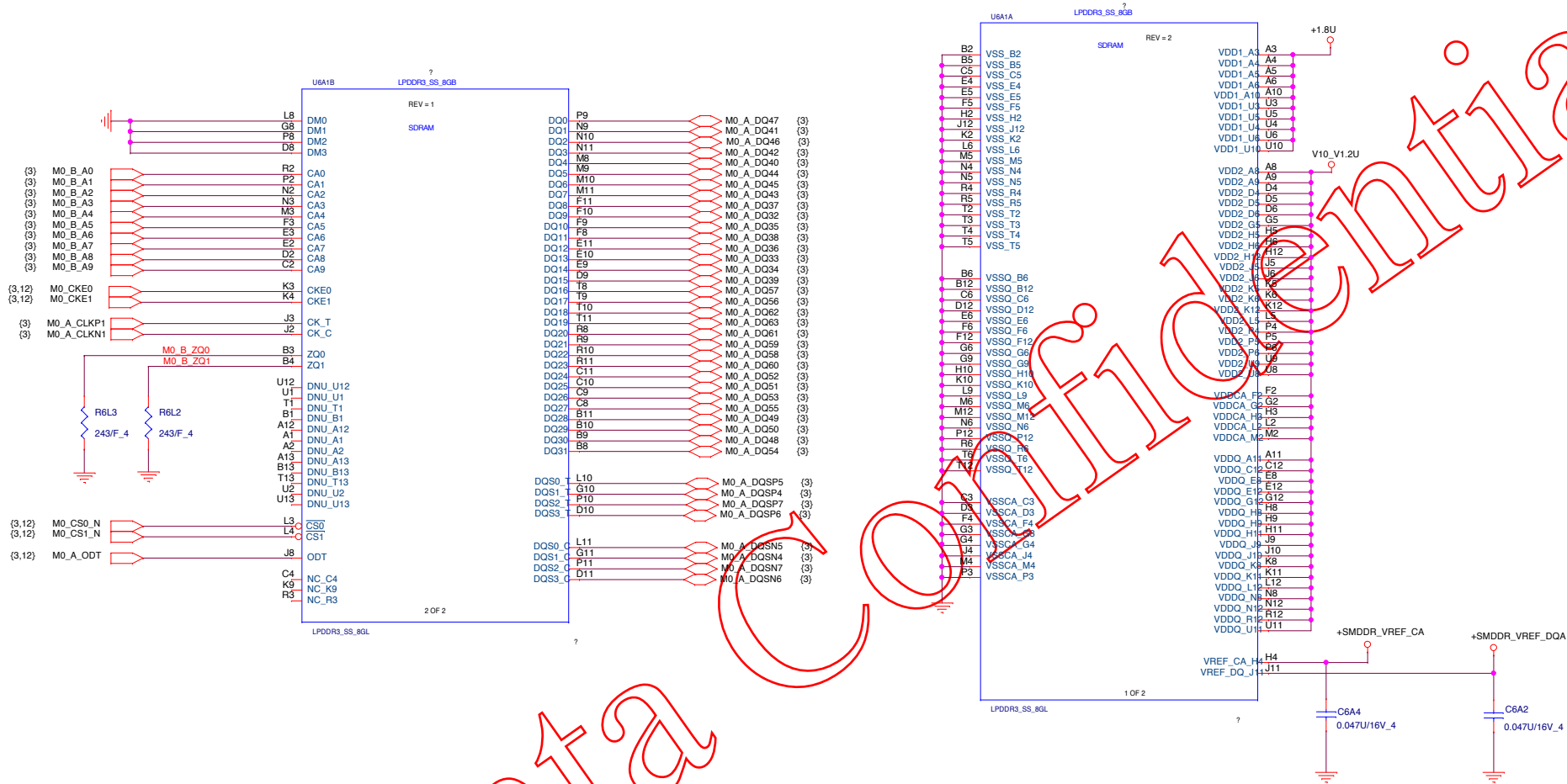


Quanta Computer Inc.

PROJECT : ZDS/ZSV

Size	Document Number	Rev
	LPDDR3 (CHA)	1A
Date:	Sunday, September 11, 2016	Sheet 12 of 42

LPDDR3 MEMORY CHANNEL A-2

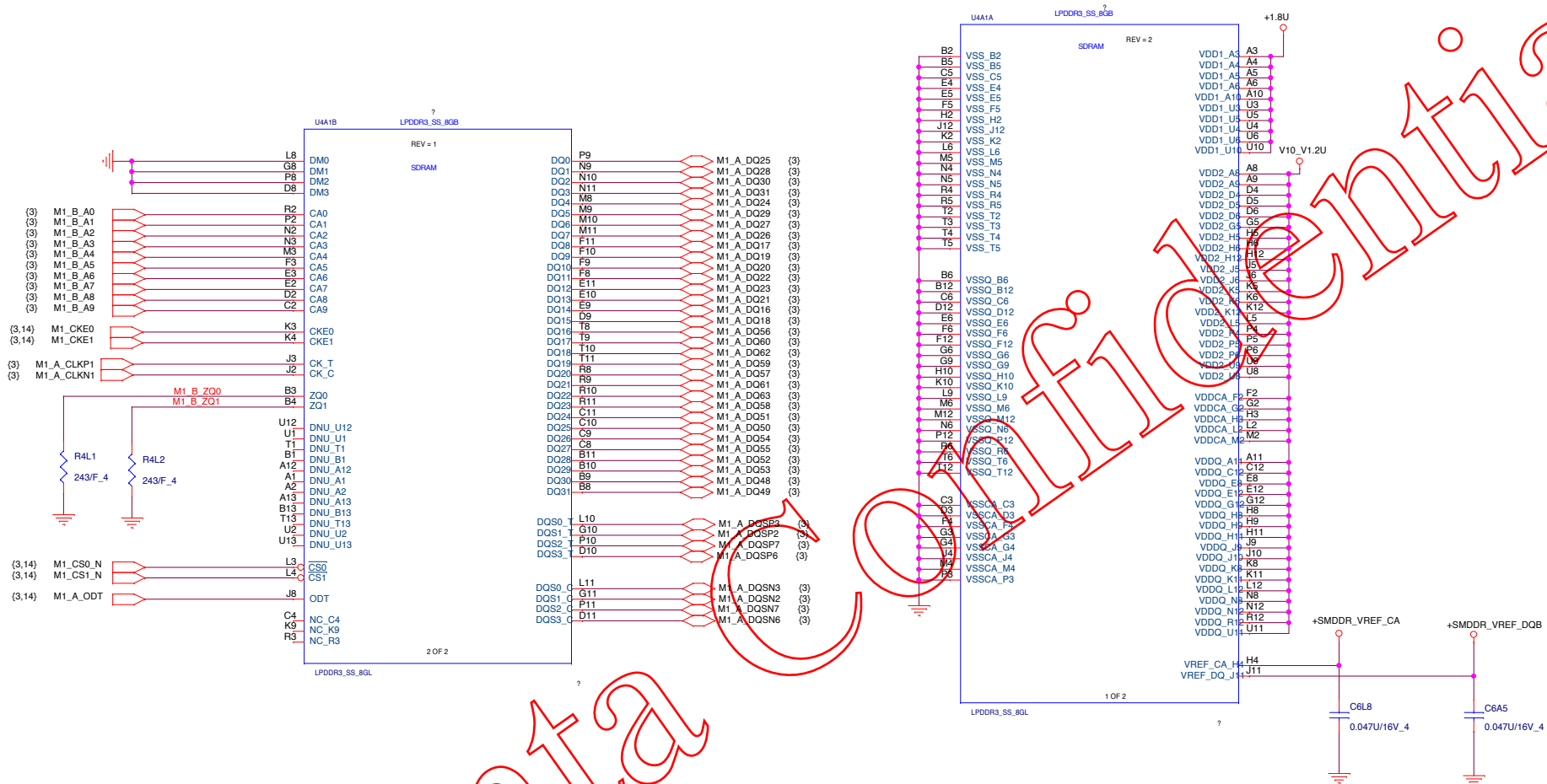


LPDDR3 MEMORY CHANNEL B-1



LPDDR3 MEMORY CHANNEL B-1

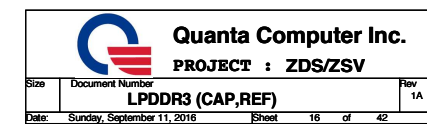
15



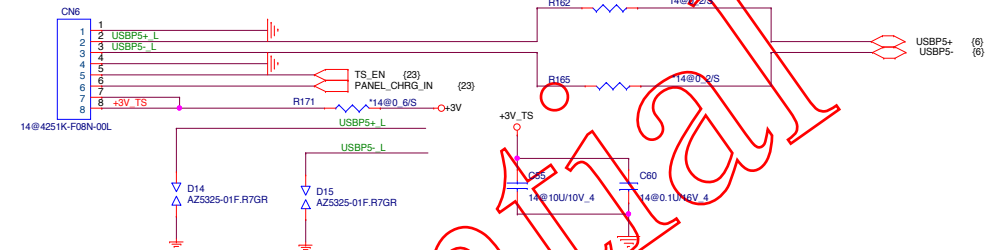
Quanta Computer Inc.
PROJECT : ZDS/ZSV

Size	Document Number	Rev
	LPDDR3 (CHB)-2	1A
Date:	Sunday, September 11, 2016	Sheet 15 of 42

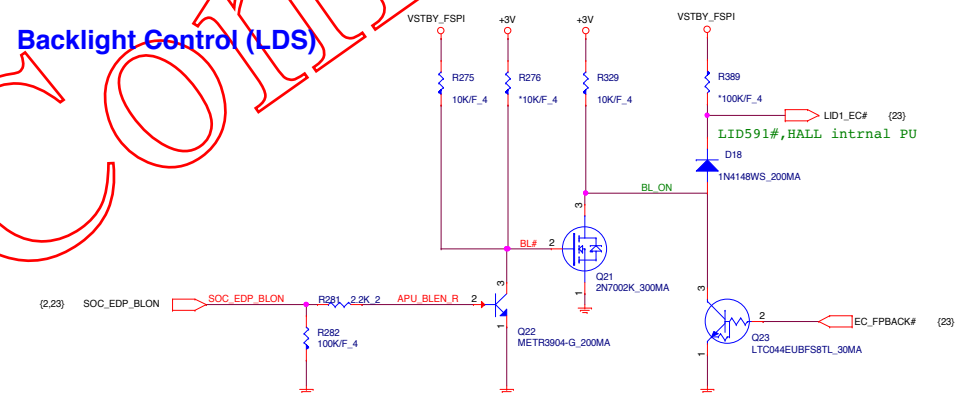
16



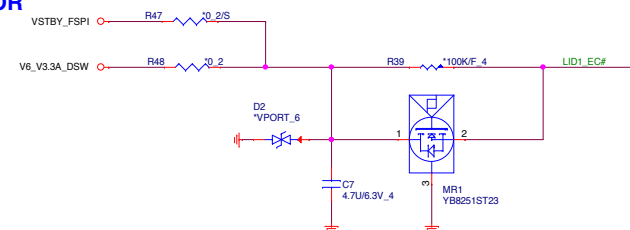
17

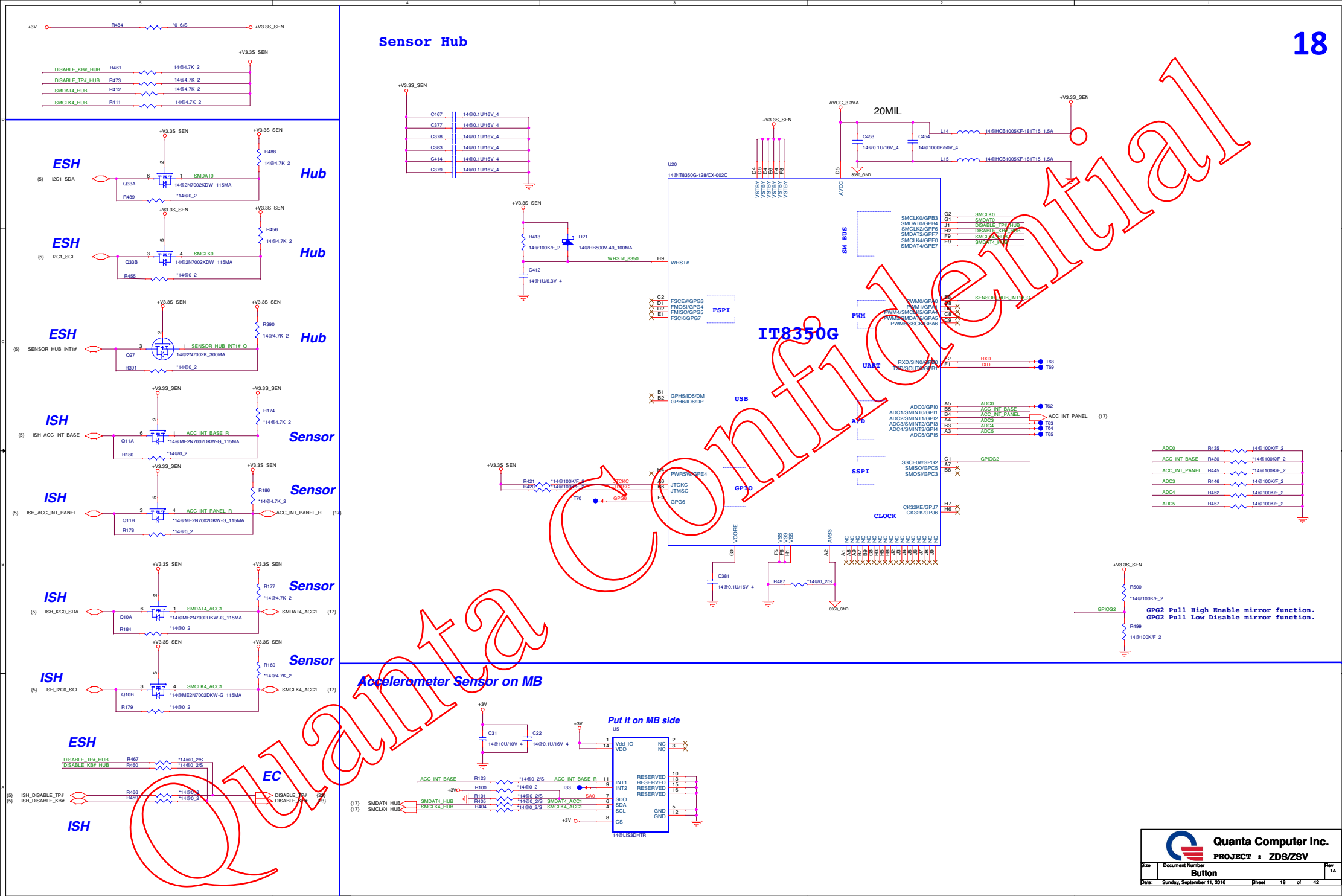
[illegible]

Backlight Control (LDS)



LID1 SENSOR

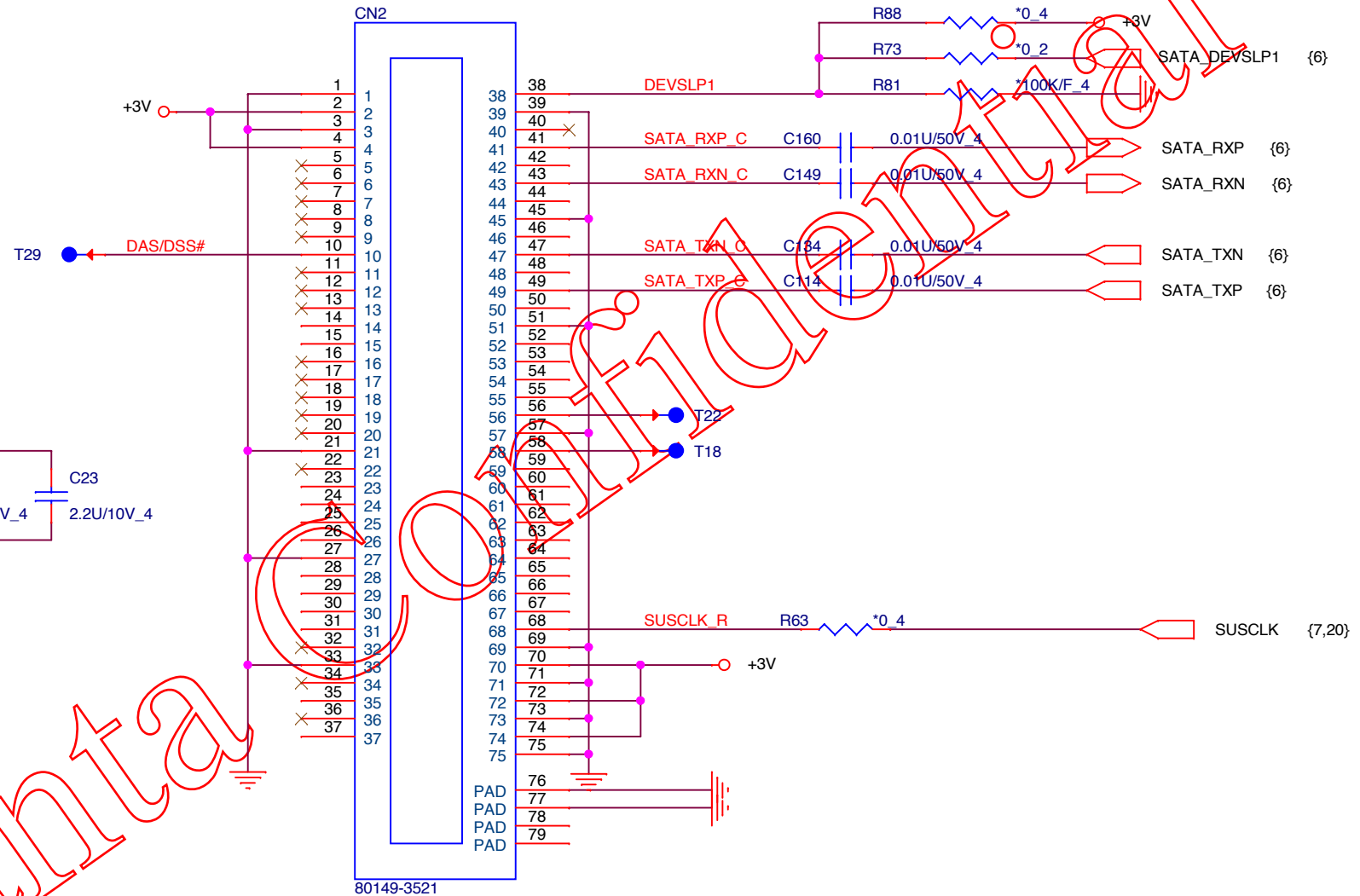
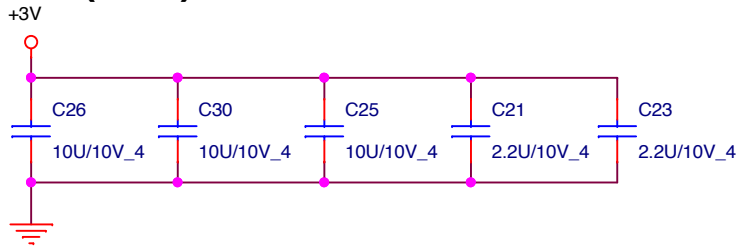




CONN: B KEY
MODULE: B KEY

Func.	CPU TX	CPU RX
PCIE2	0.1uF	0ohm
PCIE3	0.22uF	0ohm
SATA	0.01uF	0.01uF
PCIE2/SATA	0.1uF	0ohm
PCIE3/SATA	0.22uF	0ohm

2.8A(Max)



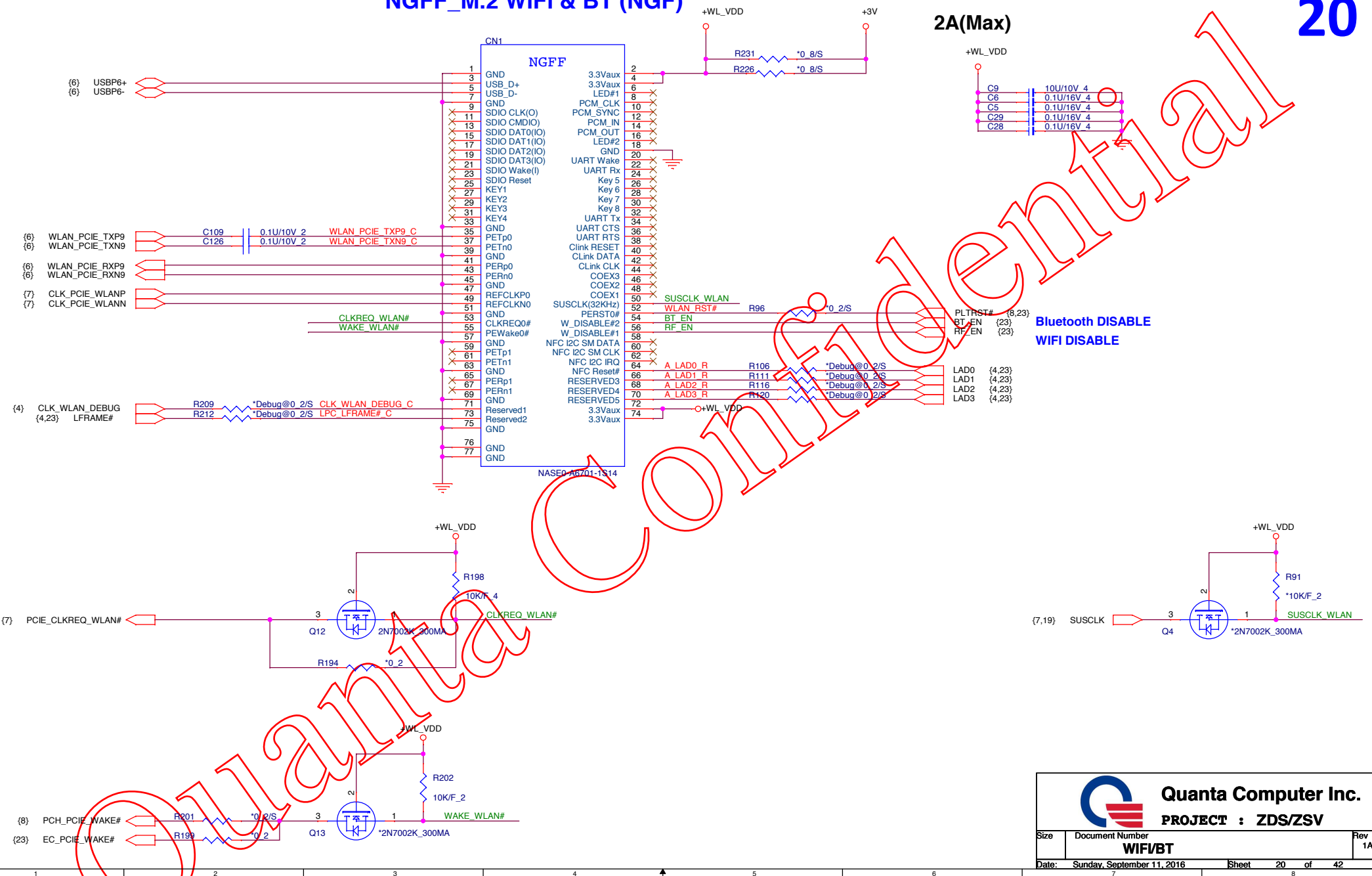
Quanta Computer Inc.

PROJECT : ZDS/ZSV

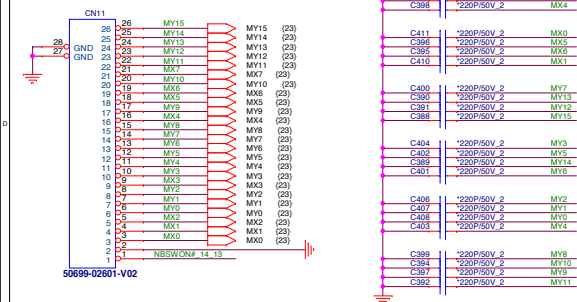
Size	Document Number	Rev
	SSD (NGFF CONN)	1A
Date:	Sunday, September 11, 2016	Sheet 19 of 42

NGFF_M.2 WiFi & BT (NGF)

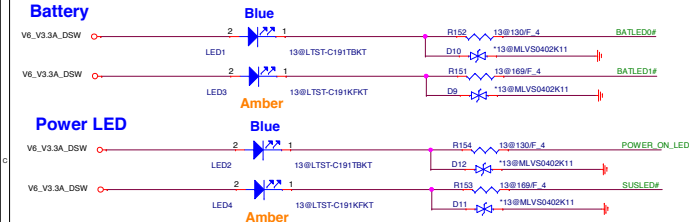
20



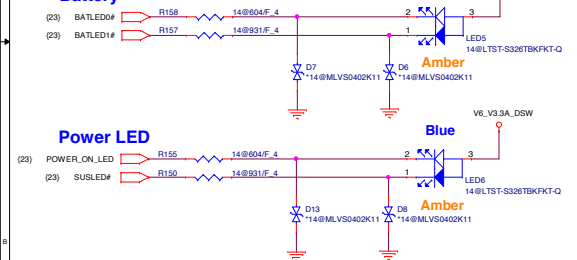
Close to KB conn



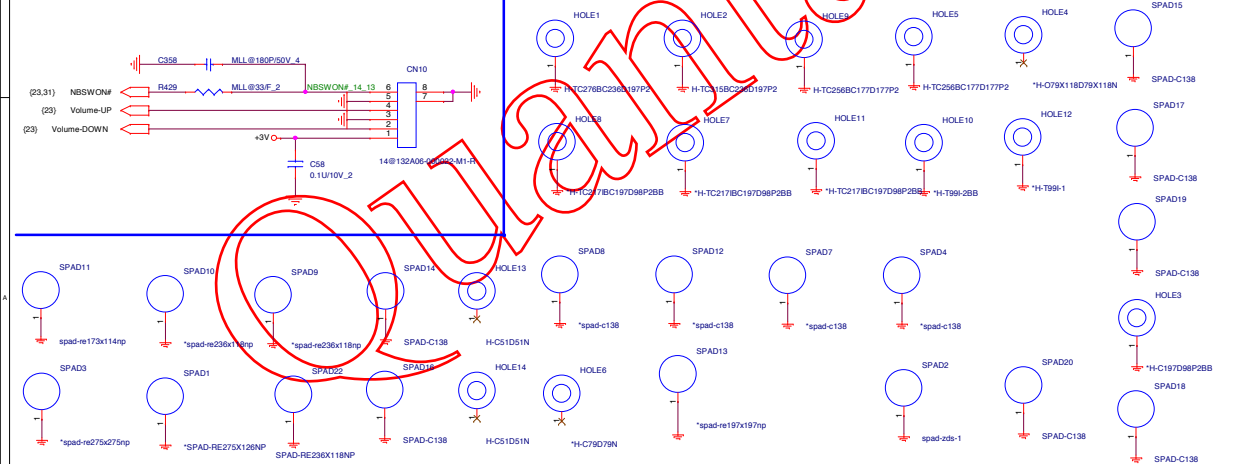
Battery



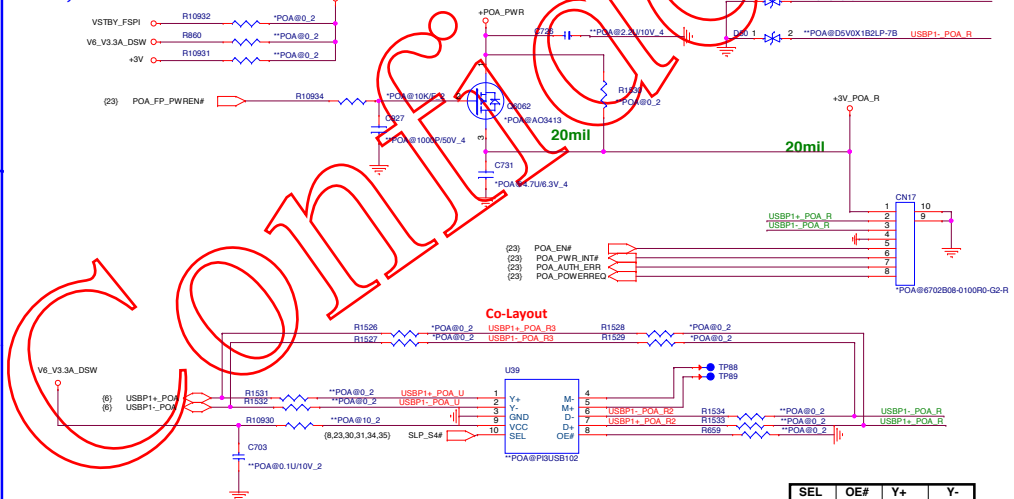
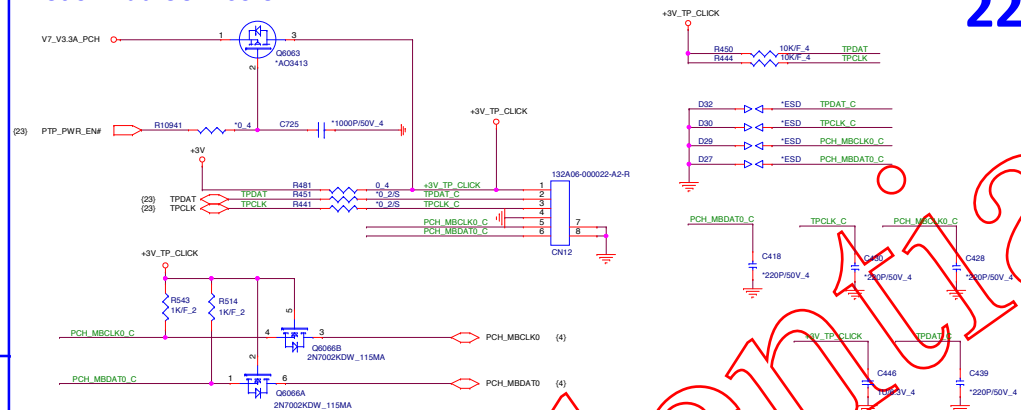
Battery



HOLE

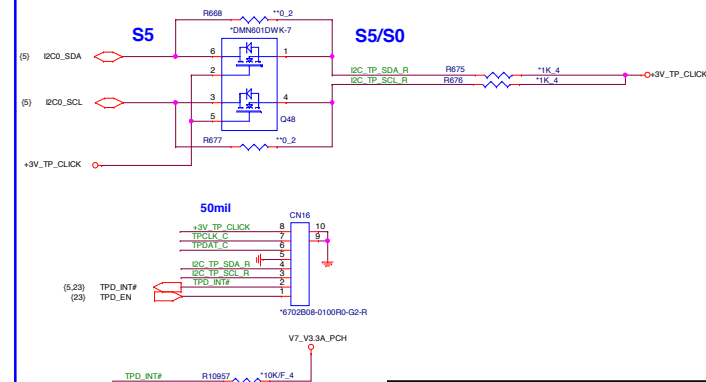


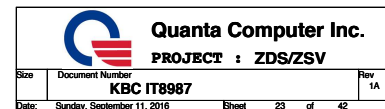
22

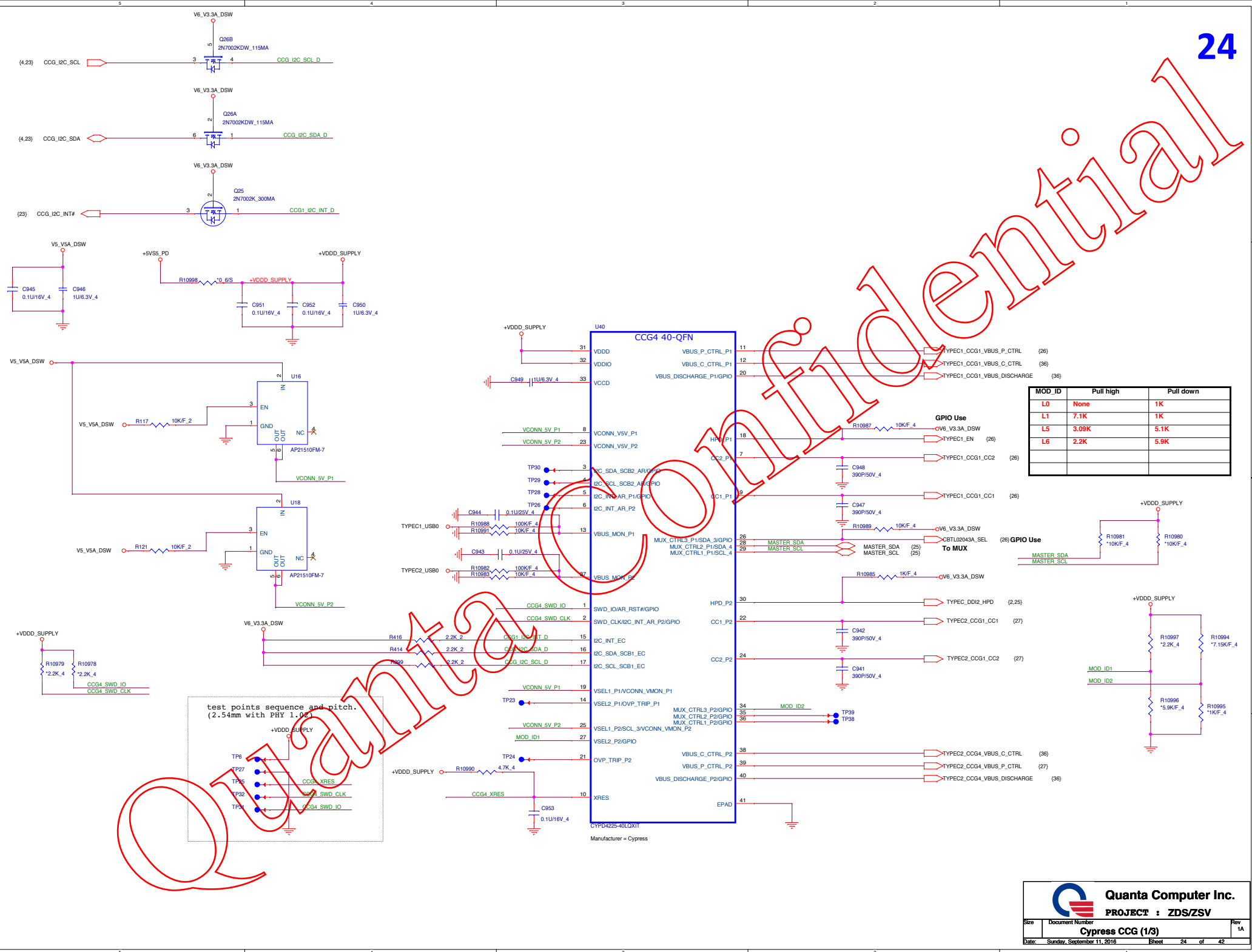


SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

Spec define: High Active







3 Level Input:
 L: LOW, internal pull down
 H: HIGH, external pull up
 M: VDD33/2, both external pull-up and pull-down

DP Source

USB3.0 HOST

DP Source

(2) DDH1_TXP0 C351 0.1U/16V 4 ML0p 9
 (2) DDH1_TXN0 C337 0.1U/16V 4 ML0n 10
 (2) DDH1_TXP3 C301 0.1U/16V 4 ML3p 18
 (2) DDH1_TXN3 C297 0.1U/16V 4 ML3n 19

(6) USB3_RXP2 C346 0.1U/16V 4 SSRXp 5
 (6) USB3_RXN2 C347 0.1U/16V 4 SSRXn 4
 (6) USB3_TXP2 C342 0.1U/16V 4 SSTXp 8
 (6) USB3_TXN2 C343 0.1U/16V 4 SSTXn 7

(2) DDH1_TXP2 C309 0.1U/16V 4 ML2p 15
 (2) DDH1_TXN2 C305 0.1U/16V 4 ML2n 16
 (2) DDH1_TXP1 C328 0.1U/16V 4 ML1p 12
 (2) DDH1_TXN1 C322 0.1U/16V 4 ML1n 13

(2) DDH1_AUXP C278 0.1U/10V 2 AUXp 24
 (2) DDH1_AUXN C279 0.1U/10V 2 AUXn 25

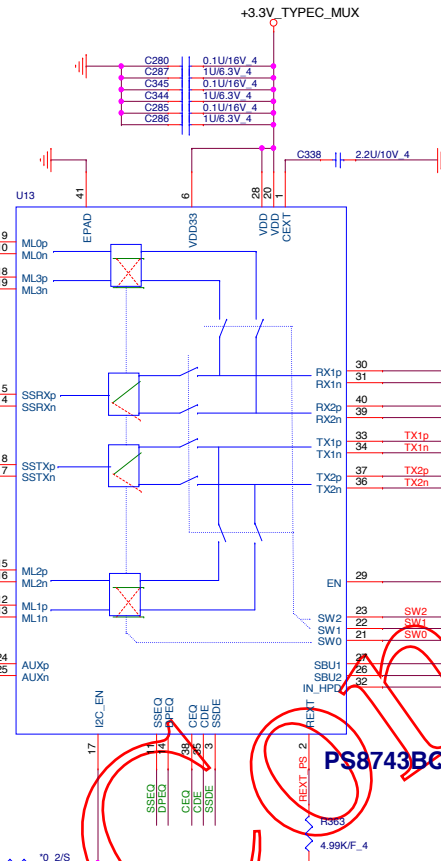
+3.3V_TYPEC_MUX

R10950 100K/F 2
 +3V
 R253 100K/F 2
 AUXn
 R252 100K/F 2
 AUXp
 +3.3V_TYPEC_MUX
 R295 0.2/S
 C282 0.1U/16V 4

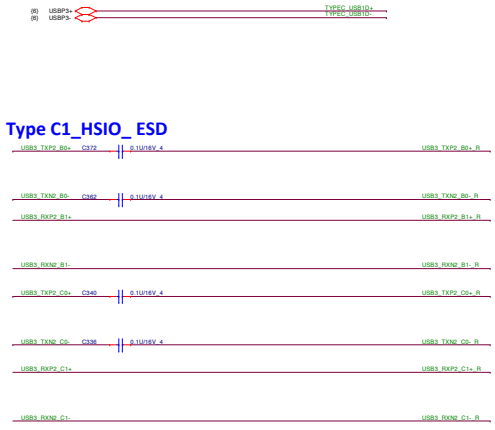
+3.3V_TYPEC_MUX
 SSEQ R318 4.7K 2
 R319 4.7K 2

+3.3V_TYPEC_MUX
 DPEQ R304 4.7K 2
 R305 4.7K 2

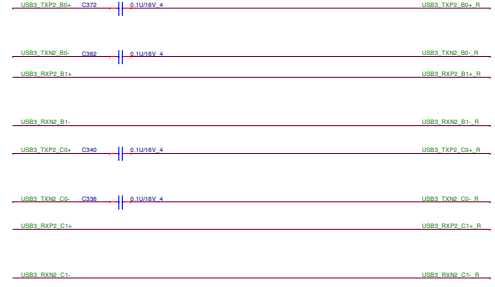
+3.3V_TYPEC_MUX
 CEQ R334 4.7K 2
 R333 4.7K 2



USB2.0 ESD

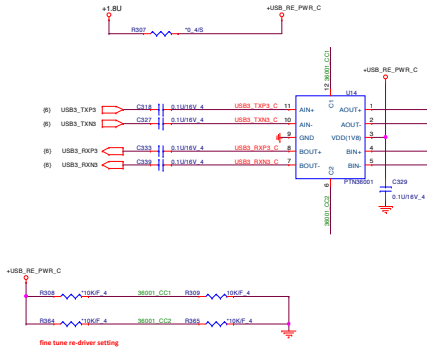


Type C1_HSIO_ESD

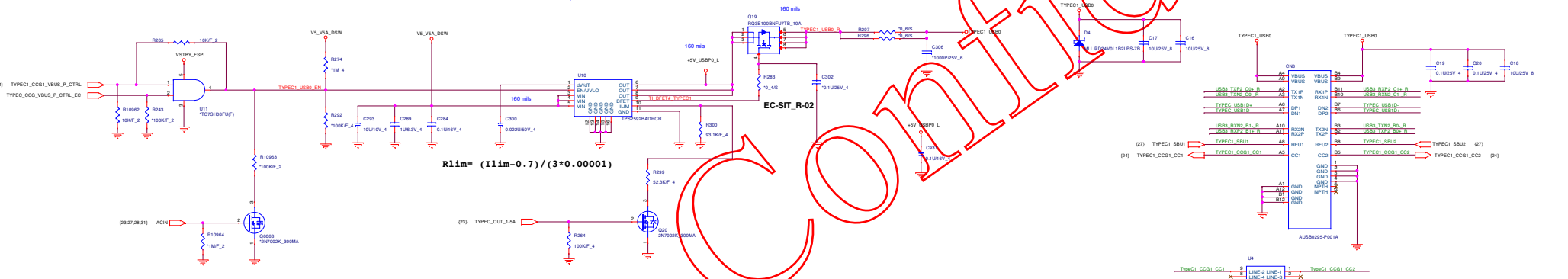
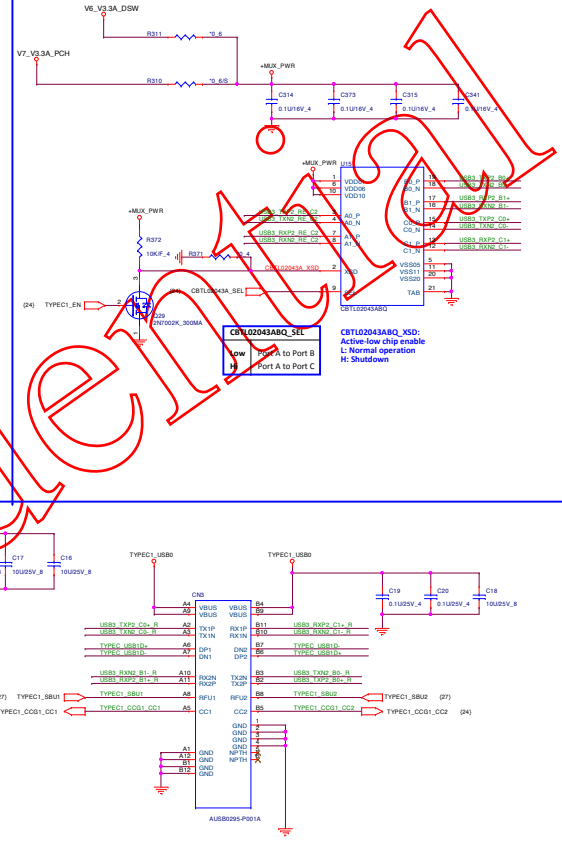


USB Type C (UTC)

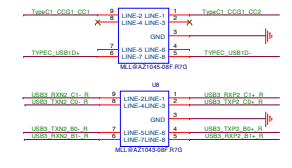
USB 3.0 redriver



Type-C MUX



$$R_{lim} = (I_{lim} - 0.7) / (3 * 0.00001)$$



Close to Type-C Conn

Quanta

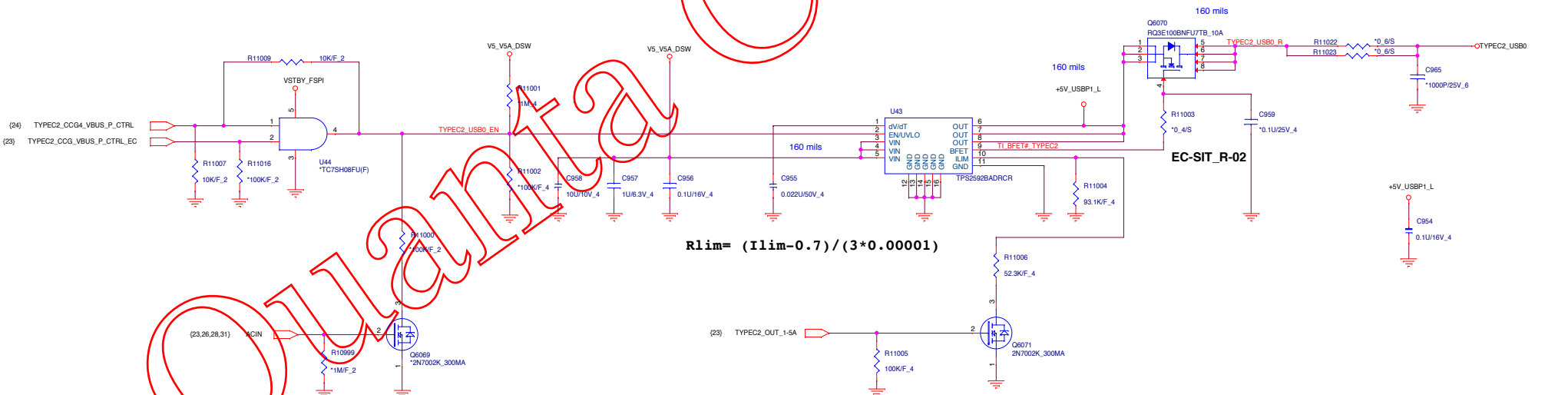
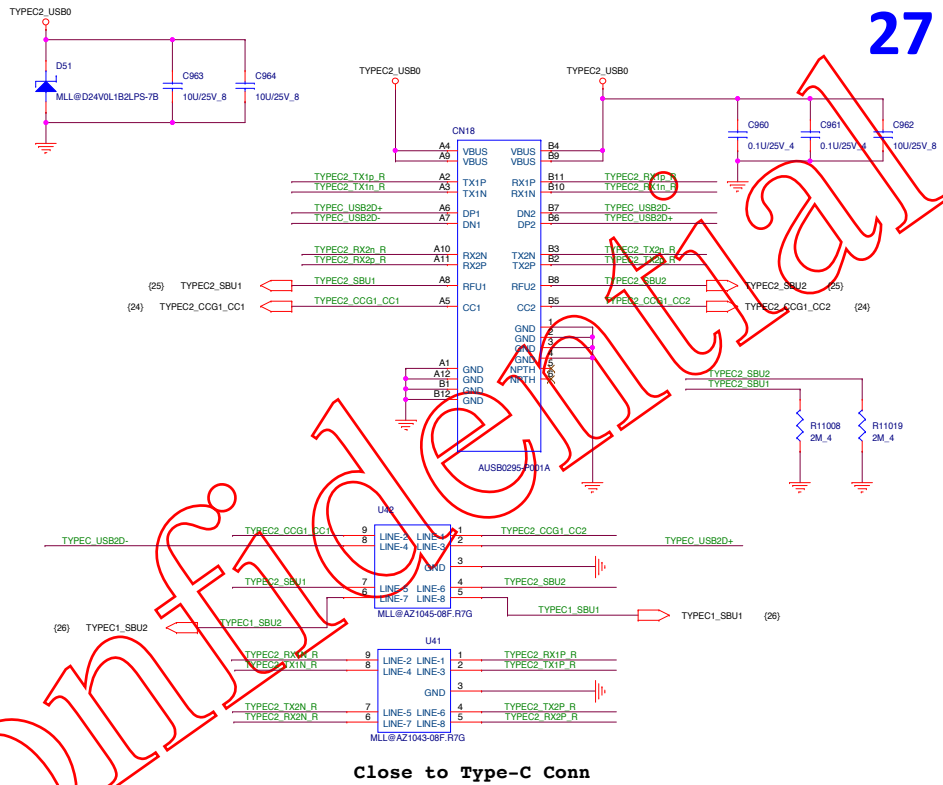
USB2.0 ESD



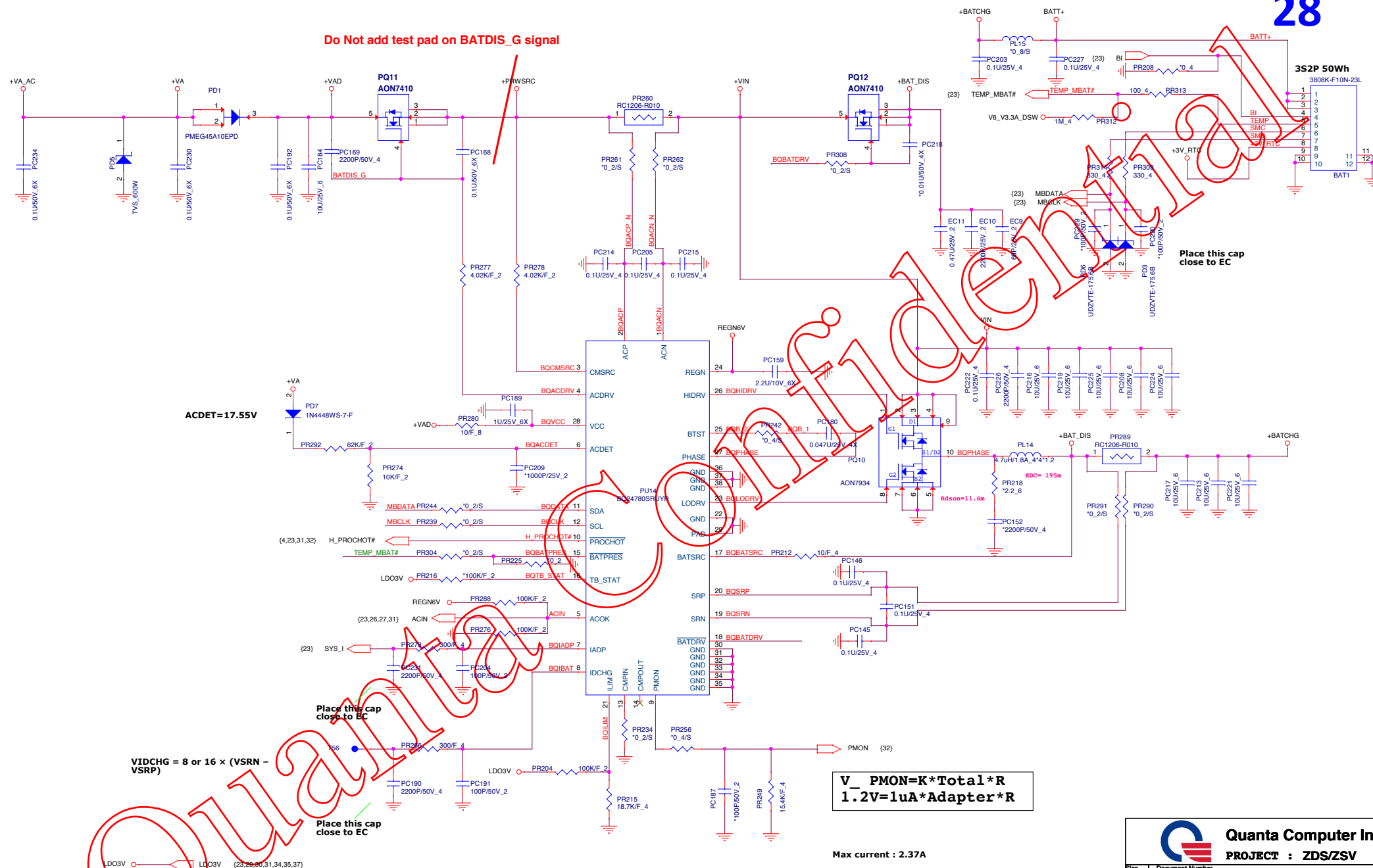
TYPE-C_HSIO_ESD

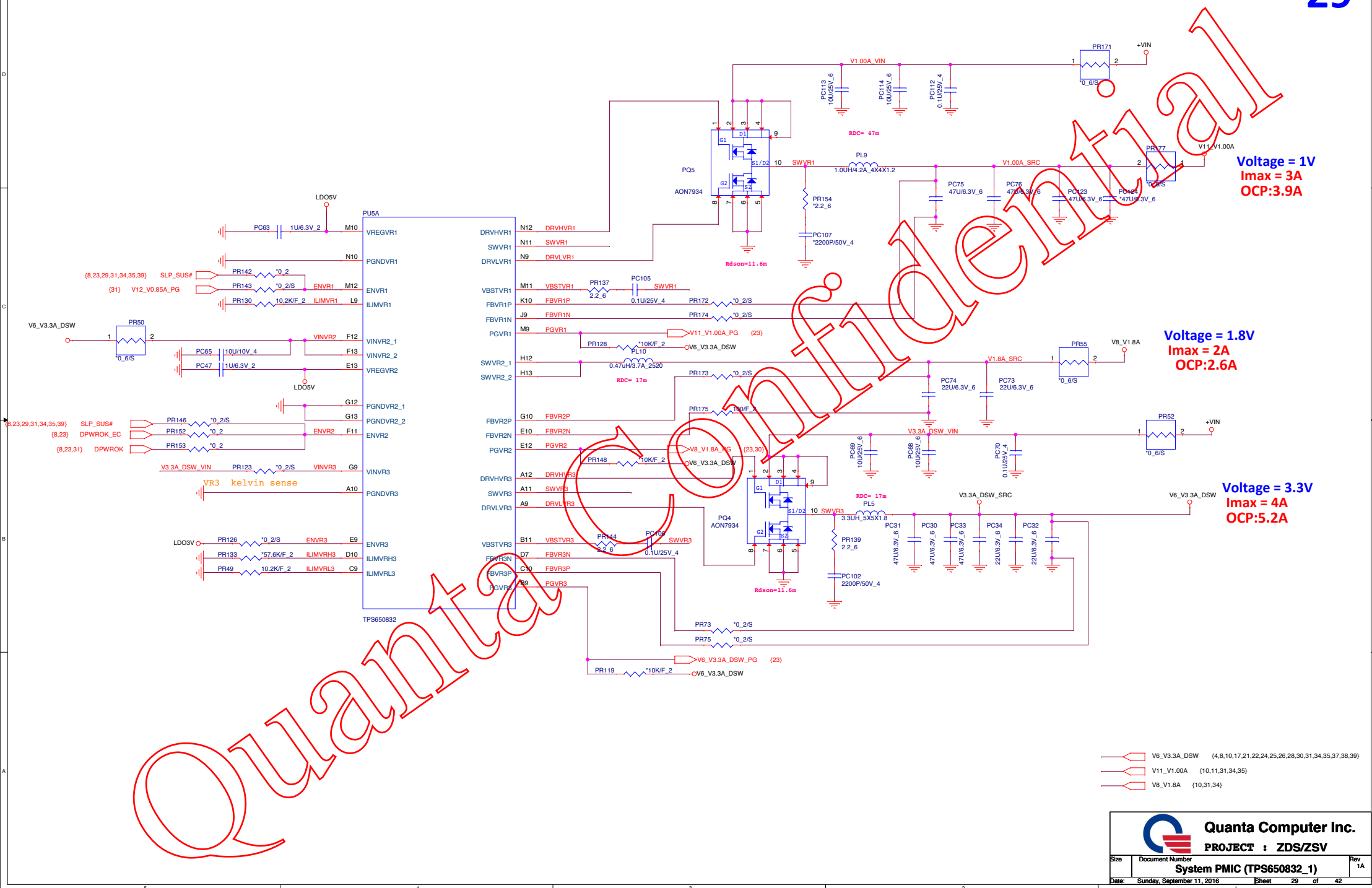


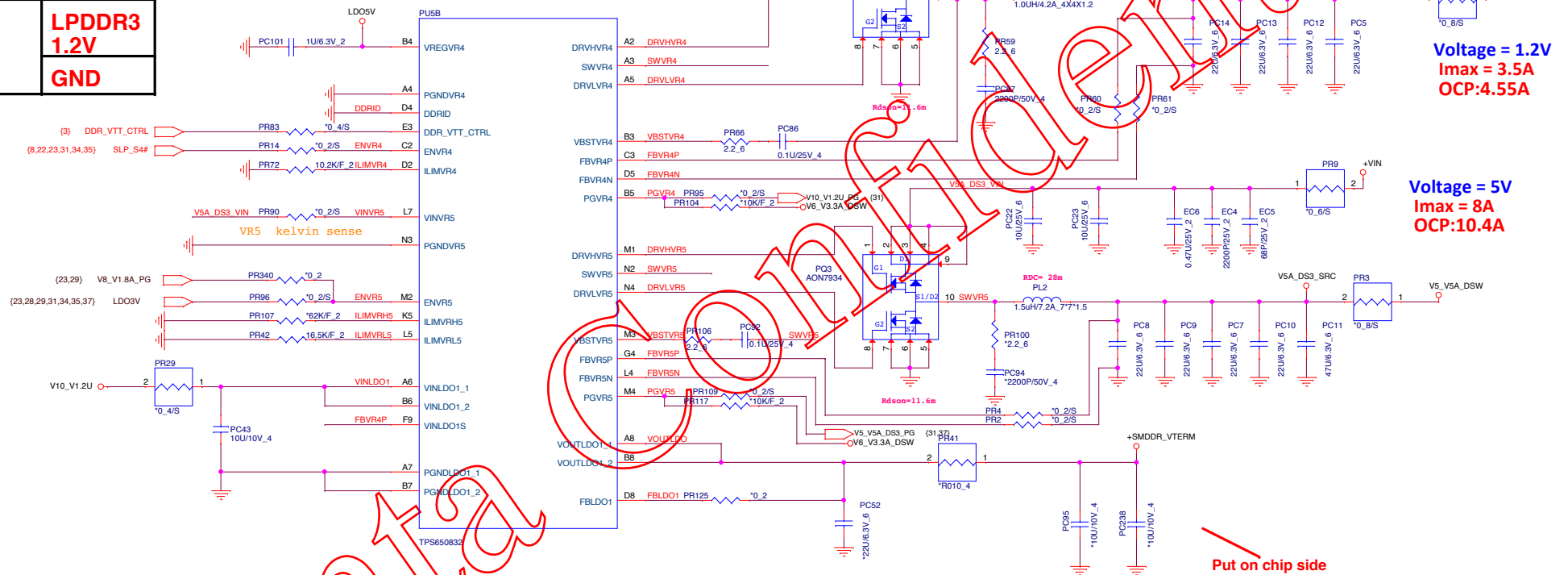
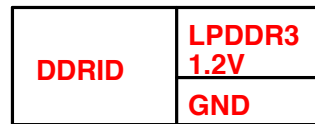
27




$$R_{lim} = (I_{lim} - 0.7) / (3 * 0.00001)$$



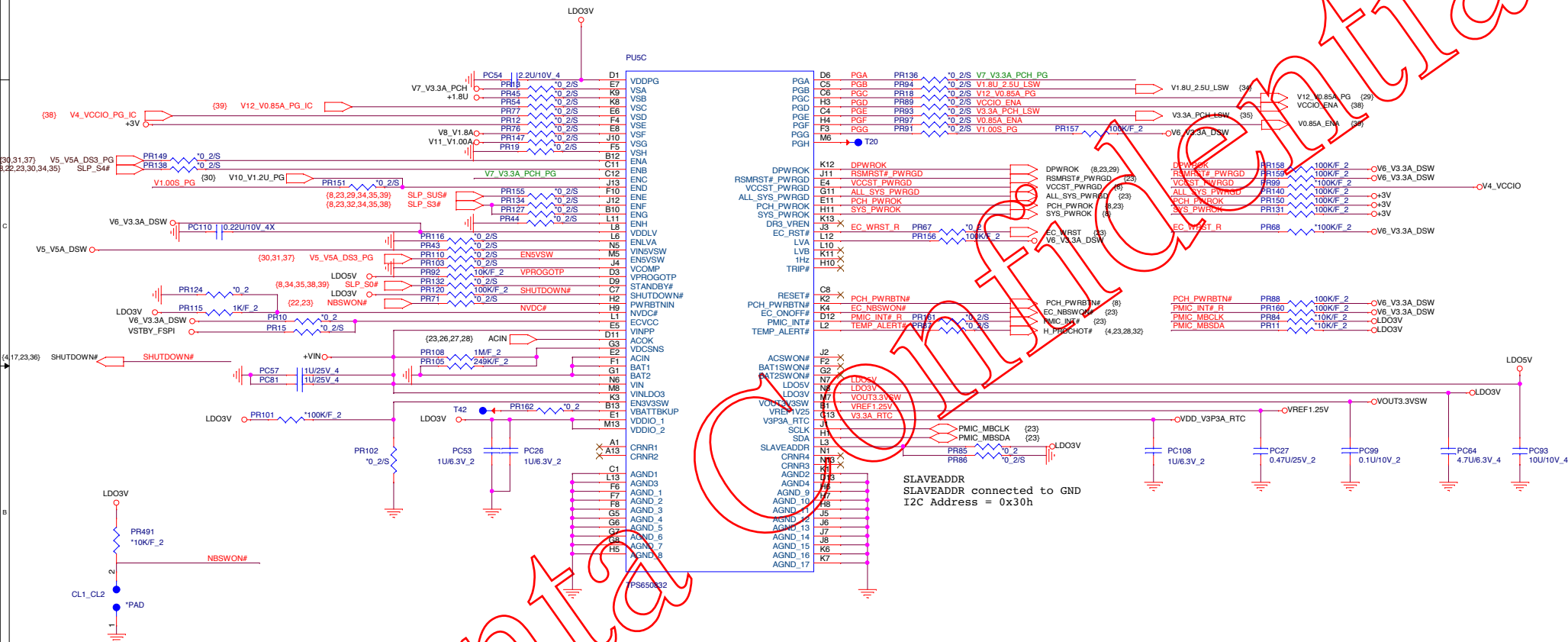




Put on chip side

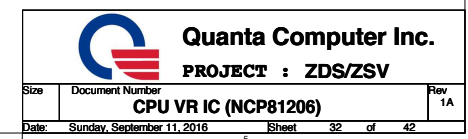
 V10_V1.2U {10,12,13,14,15,16,34}

 +SMDDR_VTERM {16}

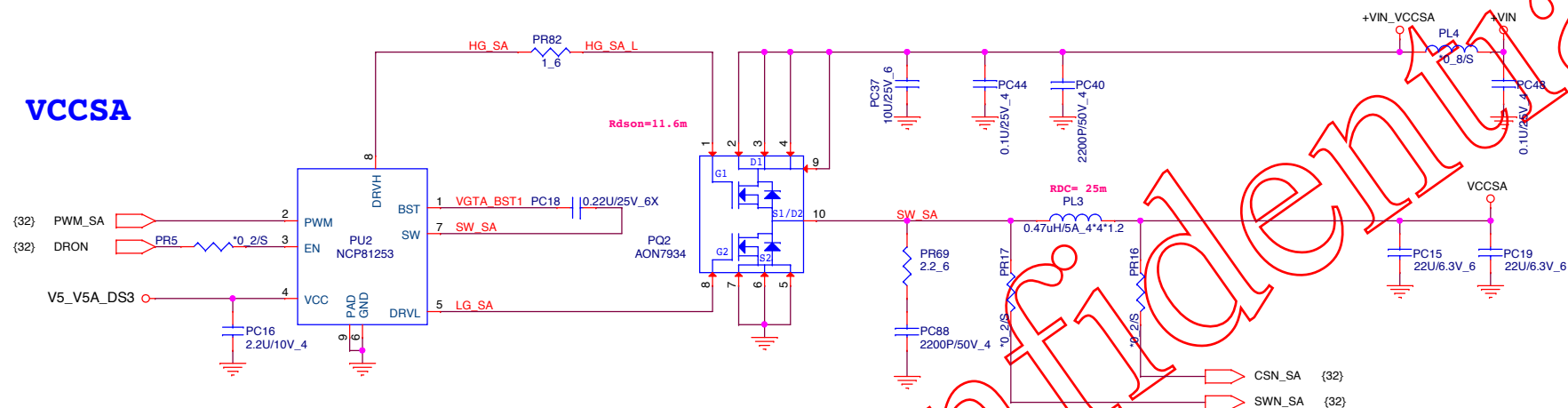


```
SLAVEADDR
SLAVEADDR connected to GND
I2C Address = 0x30h
```

LDO3V LDO3V {23,28,29,30,34,35,37}



VCCSA



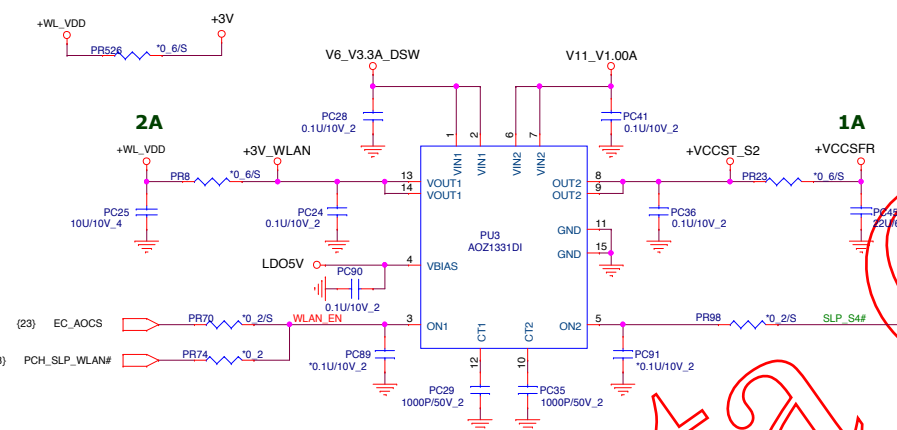
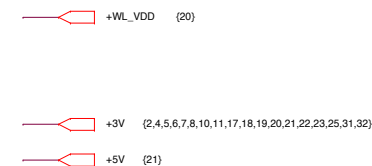
VCCSA
TDC:4A
EDP:5.2A

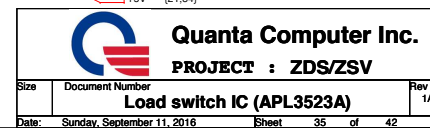
33



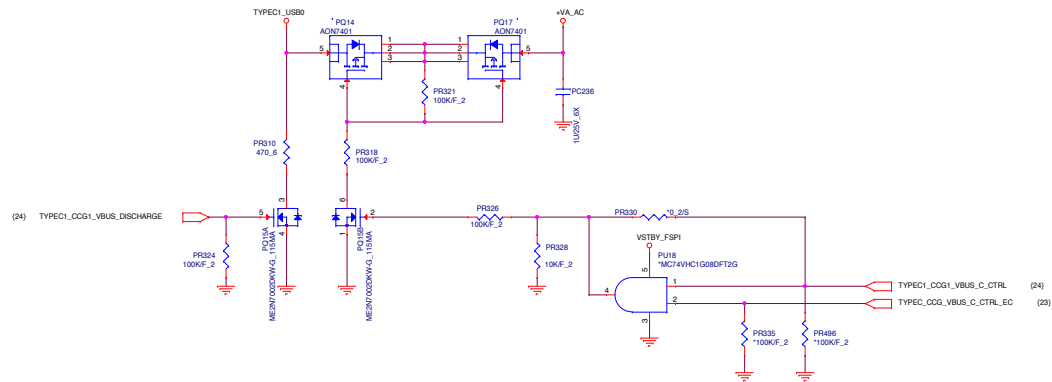
Quanta Computer Inc.
PROJECT : ZDS/ZSV

Size	Document Number +VCCSA (NCP81253)	Rev 1A
Date:	Sunday, September 11, 2016	Sheet 33 of 42

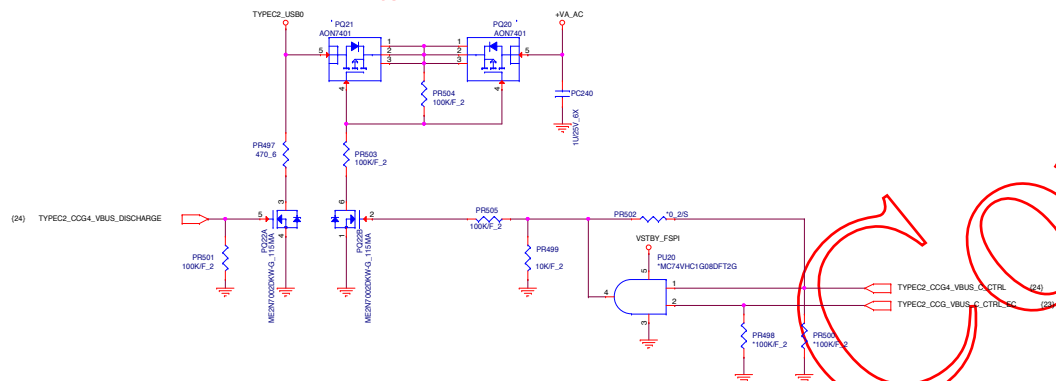




For TypeC PORT1

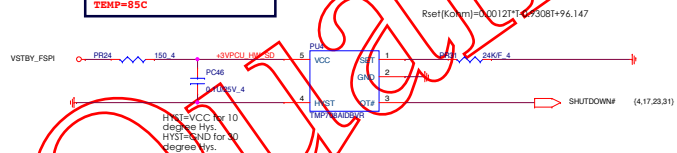


For TypeC PORT2



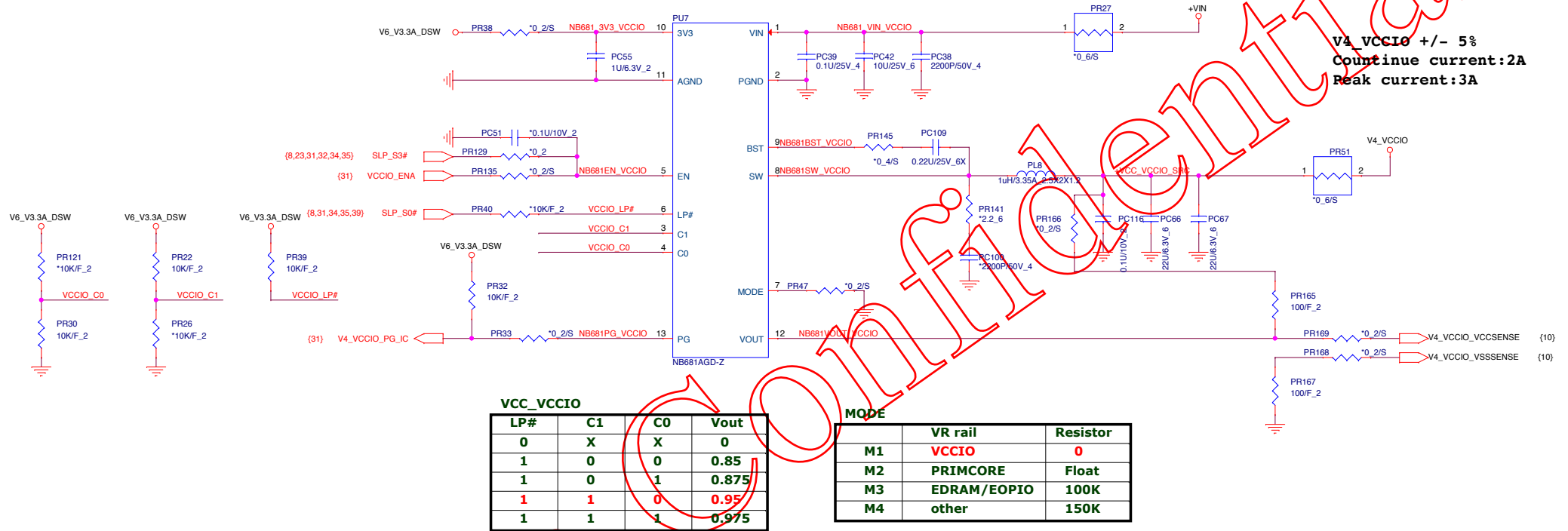
Thermal protection

For thermal protect point
Note placement position
TEMP=85C



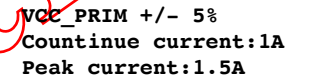


(17,21,28,29,30,31,32,33,39) +VIN
(2,7,10,31) V4_VCCIO



Quanta Computer Inc.
PROJECT : ZDS/ZSV

Size Document Number Rev 1A
+VCC_VCCIO (NB681)
Date: Sunday, September 11, 2016 Sheet 38 of 42

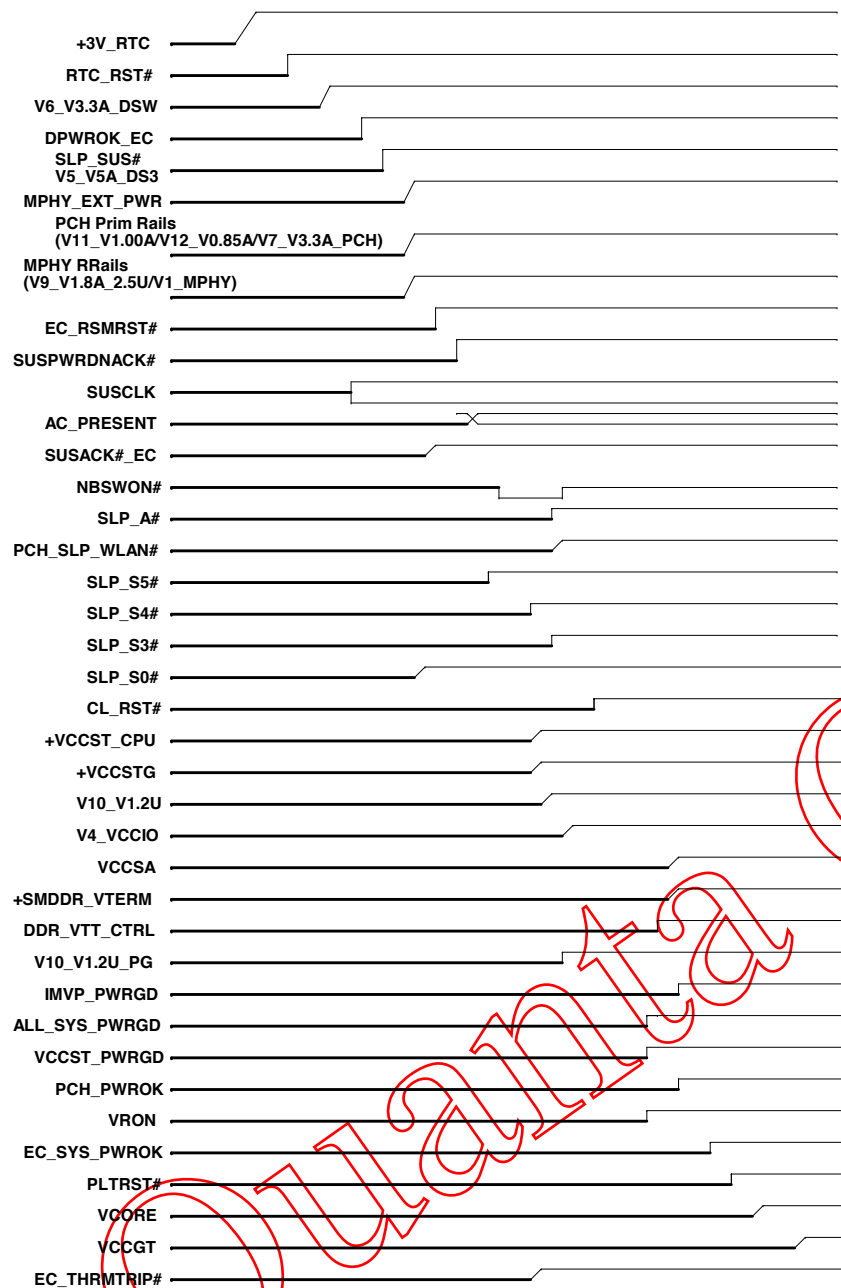


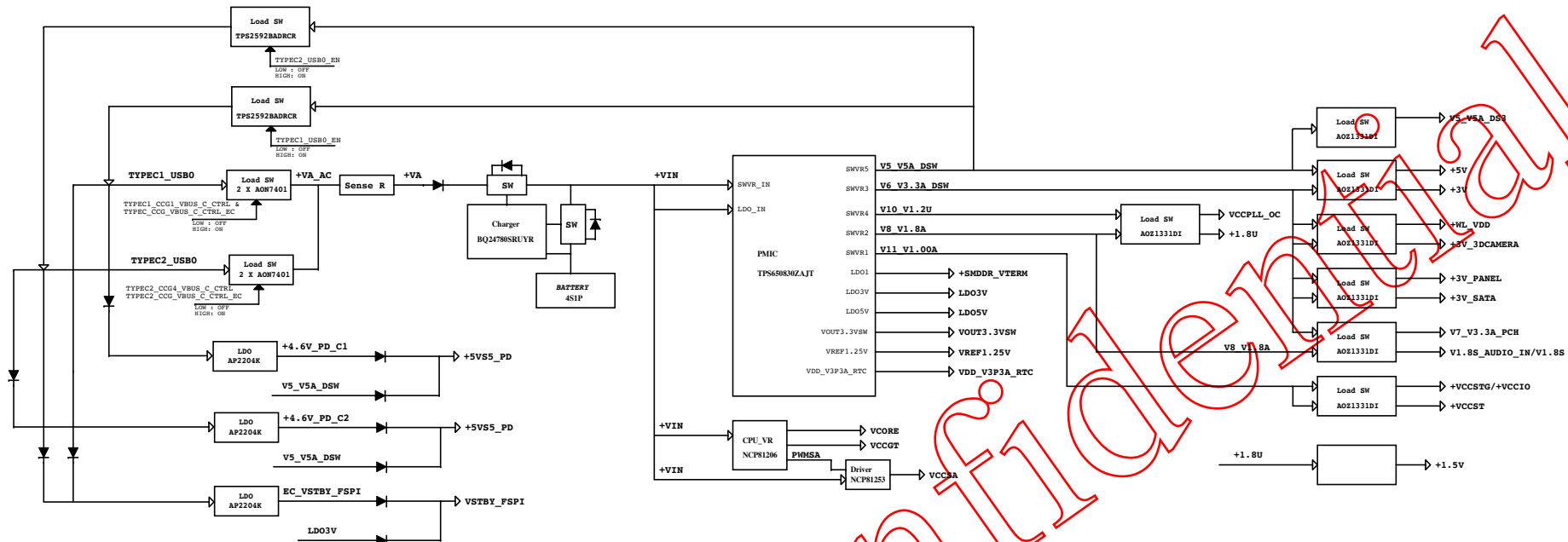
LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.85
1	0	1	0.9
1	1	0	0.95
1	1	1	1.00

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

Power up sequence

40





Quanta

Confidential

Model	Date	CHANGE LIST
ZDS/ZDV REV:A	4/27	1. FIRST RELEASED
ZDS/ZDV REV:B	6/1	1. Change PR284/PR193/PR247/PR283/PR273/PR187/PR240 Value for CPU transient and load line 2. Add PR492/PR493/PU19/PR495 for sequence 3. Add Q6064 for EC read PCH temperature 4. Change R52/R54 Value from 4.7K to 1K ohm for Touch pad 5. Add R10592/R10591/D39 for RTC voltage 6. Change R291/R47 PU netname from VSTBY_FSP to VSTBY_FSPI for netname wrong 7. Add R10953/R10954/R10955/R10956 for separate Boxster and Dino MIC signals 8. Stuff R309 for USB RX
ZDS/ZDV REV:C1	7/10	1. Remove R28 / Add R10971 to link V7_V3.3A_PCH for leakage current issue 2. Remove R133,R130,R128,R124,R67,R61 and Add R10967,R10966,R10968 to link V7_V3.3A_PCH for leakage current issue 3. Reverse POA/PBA circuit for customer requirement 4. Remove R32,R113 and Add Add R10970 to link V7_V3.3A_PCH for leakage current issue 5. Change C81/C80/C83//C96/C228/C484/C485/C483/C487/C488 Value to 47U/4V_8H095 for ID height-Z limitation 6. Add C51/C52/C53/C121/C185/C199/C225/C64//C65/C66/C235/C161/C233 for VCCGT voltage stable 7. Add C259/C267 for V4_VCCIO voltage stable 8. Add C940/C939/C938/C937/C936/C935/C934/C312/C425/C426 for V10_V1.2U voltage stable 9. Change 13" ZDS Dual MIC connector from 4pin to 8 pin for FA issue 10. Add D14/D15 for ESD fail 11. Remove R391/R455/R489 and mount Q33/Q27/R390/R456/R488 for leakage current issue 12 Change Audio Jack CN5 from 5 pin to 7 pin for noise issue 13. Change R151/R152/R153/R154/R150/R155/R157/R158 Value for LED brightness issue 14. Change PR292/PR274 Value for ACDet 15. Change PL5 from 1UH to 3.3UH for Noise issue
ZDS/ZDV REV:C2	7/27	1. Change PD circuit from CCG2 to CCG4 for support PD*2
ZDS/ZDV REV:C3	8/10	1. Del R330,R314,R323,R341,R291 and add Q6072,R332,R337,R505 to V7_V3.3A_PCH for S5 leakage current issue 2. Change R150,R151,R152,R153,R154,R157 PN to fine tune LED brightness for ME ID Len change Lens color issue 3. Del R10980,R10981,R298,Q18,R311 and add R285,R273,R266,R259,R260,R295,R310,C282 and change Change U16,U18,R117,R121 to V5_V5A_DSW for S4 resume TYPE C device detect detect issue
ZDS/ZDV REV: Ramp	8/22	1. Change 0 ohm to shortpad